



ByteBlaster II Parallel Port Download Cable

August 2003, Version 2.0

Data Sheet

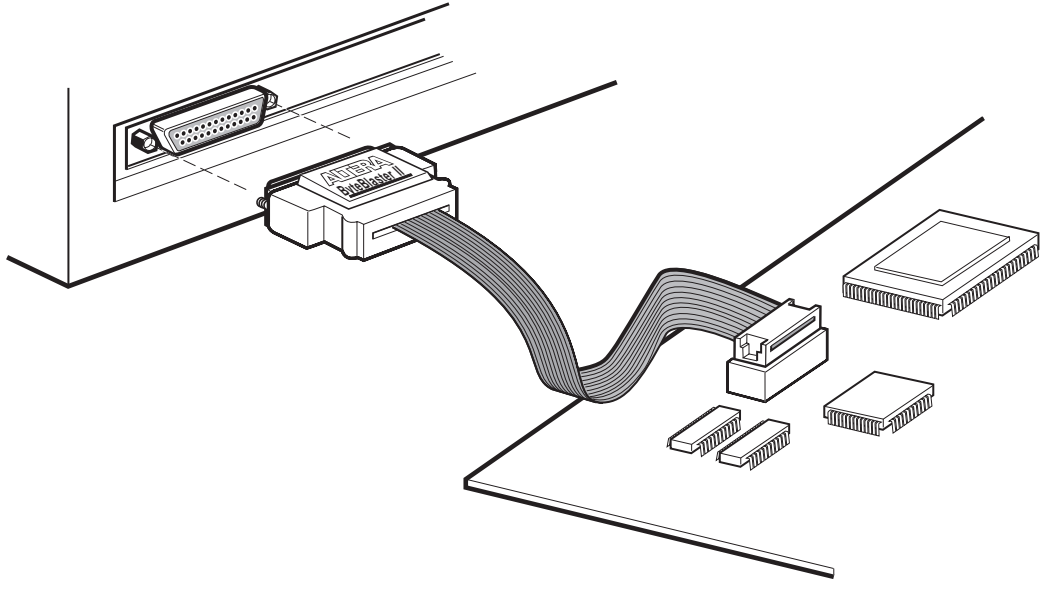
Features

- Allows PC users to perform the following functions:
 - Program MAX[®] 9000, MAX 7000S, MAX 7000AE, MAX 7000B, MAX 3000A, advanced configuration (EPC2, EPC4, EPC8, and EPC16) and serial (EPCS) configuration devices in-system
 - Configure Stratix[™], Stratix[™] GX, Cyclone[™], APEX[™] II, APEX 20K (including APEX 20K, APEX 20KE, and APEX 20KC), ACEX[®] 1K, Mercury[™], FLEX[®] 10K (including FLEX 10KA and FLEX 10KE), FLEX 8000, FLEX 6000, and Excalibur[™] devices.
- Supports target systems using 5.0 V TTL, 3.3 V LVTTTL/LVCMOS, and single-ended I/O standards from 3.3 V down to 1.8 V.
- Provides a fast and low-cost method for in-system programming
- Supported by the Altera[®] Quartus[®] II development software
- Interfaces with a standard 25-pin parallel port on PCs
- Uses a 10-pin circuit board connector, which is compatible with the ByteBlasterMV[™] parallel port cable and BitBlaster[™] serial download cable
- Supports SignalTap[®] II logic analysis in the Quartus II software

Functional Description

The ByteBlaster II parallel port download cable (ordering code: PL-BYTEBLASTER2) interfaces to a standard PC parallel port (also known as an LPT port). This cable drives configuration data from the PC to Stratix, Stratix GX, Cyclone, APEX II, APEX 20K (including APEX 20K, APEX 20KE, and APEX 20KC), ACEX 1K, Mercury, Excalibur, FLEX 10K (including FLEX 10KA and FLEX 10KE), FLEX 8000, and FLEX 6000 devices, as well as programming data to MAX 9000, MAX 7000S, MAX 7000AE, MAX 7000B, MAX 3000A devices and EPC/EPCS configuration devices. Because design changes are downloaded directly to the device, prototyping is easy and multiple design iterations can be accomplished in quick succession. See [Figure 1](#).

Figure 1. ByteBlaster II Parallel Port Download Cable



Download Modes

The ByteBlaster II cable provides three download modes:

- Active Serial (AS) mode—Used for programming serial (EPCS) configuration devices.
- Passive serial (PS) mode—Used for configuring Stratix, Stratix GX, Cyclone, APEX II, APEX 20K, Mercury, ACEX 1K, Excalibur, FLEX 10K, FLEX 8000, and FLEX 6000 devices
- JTAG mode—Industry-standard Joint Test Action Group (JTAG) interface for programming or configuring Stratix, Stratix GX, Cyclone, APEX II, APEX 20K, Mercury, ACEX 1K, Excalibur, FLEX 10K, MAX 9000, MAX 7000S, MAX 7000AE, MAX 7000B, and MAX 3000A devices, and EPC configuration devices.

ByteBlaster II Connections

The ByteBlaster II cable has a 25-pin male header that connects to the PC parallel port, and a 10-pin female plug that connects to the circuit board. Data is downloaded from the PC's parallel port through the ByteBlaster II cable to the circuit board via the connections discussed in this section.



The ByteBlaster II V_{CC} pin must be connected to a specific voltage for the device being programmed (Table 1). Connect pull-up resistors to the same power supply as the ByteBlaster II V_{CC} .

Family	ByteBlaster II VCC Voltage Required
MAX 7000S	5 V
MAX 7000AE, MAX 3000A	3.3 V
MAX 7000B	2.5 V
Stratix, Stratix GX	As specified by V_{CCSEL}
Cyclone, APEX II, APEX 20K, Mercury	As specified by V_{CCIO}
FLEX 10K, FLEX 8000, FLEX 6000	5 V
FLEX 10KE	2.5 V
FLEX 10KA, FLEX 6000A	3.3 V
EPC2	5 V or 3.3 V
EPC4, EPC8, EPC16	3.3 V
EPCS1, EPCS4	3.3 V

ByteBlaster II Header & Plug Connections

The 25-pin male header connects to a parallel port with a standard parallel cable. Table 2 identifies the pins and the download modes.

Pin	AS Mode Signal Name	PS Mode Signal Name	JTAG Mode Signal Name
2	DCLK	DCLK	TCK
3	nCONFIG	nCONFIG	TMS
4	nCS	–	–
5	nCE	–	–
8	ASDI	DATA0	TDI
11	CONF_DONE	CONF_DONE	TDO
13	DATAOUT	nSTATUS	–
15	nVCC Detect	nVCC Detect	nVCC detect
18 to 25	GND	GND	GND

The 10-pin female plug connects to a 10-pin male header on the circuit board containing the target device(s). Figure 2 shows the dimensions of the female plug.

Figure 2. ByteBlaster II 10-Pin Female Plug Dimensions

Dimensions are shown in inches. The spacing between pin centers is 0.1 inch.

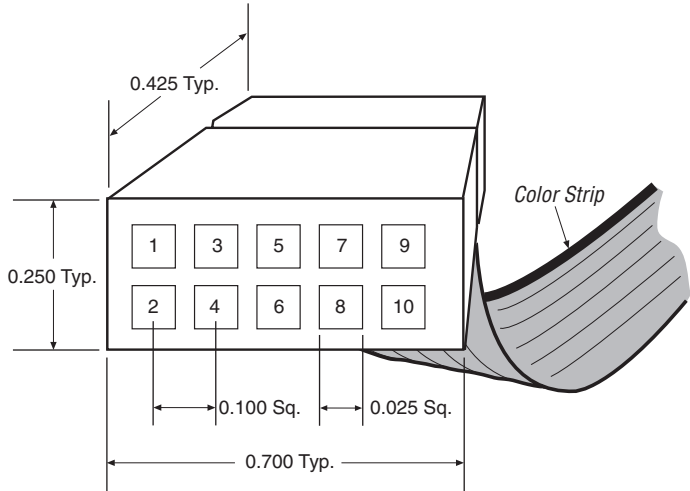



Table 3 identifies the 10-pin female plug's pin names for the corresponding download mode.

Table 3. ByteBlaster II Female Plug's Pin Names & Download Modes

Pin	AS Mode		PS Mode		JTAG Mode	
	Signal Name	Description	Signal Name	Description	Signal Name	Description
1	DCLK	Clock Signal	DCLK	Clock signal	TCK	Clock signal
2	GND	Signal Ground	GND	Signal ground	GND	Signal ground
3	CONF_DONE	Configuration Done	CONF_DONE	Configuration Done	TDO	Data from device
4	VCC	Power Supply	VCC	Power supply	VCC	Power supply
5	nCONFIG	Configuration Control	nCONFIG	Configuration control	TMS	JTAG state machine control
6	nCE	Cyclone Chip Enable	–	No connect	–	No connect
7	DATAOUT	Active Serial Data Out	nSTATUS	Configuration status	–	No connect
8	nCS	Serial Configuration Device Chip Select	–	No connect	–	No connect
9	ASDI	Active Serial Data In	DATA0	Data to device	TDI	Data to device
10	GND	Signal Ground	GND	Signal ground	GND	Signal ground

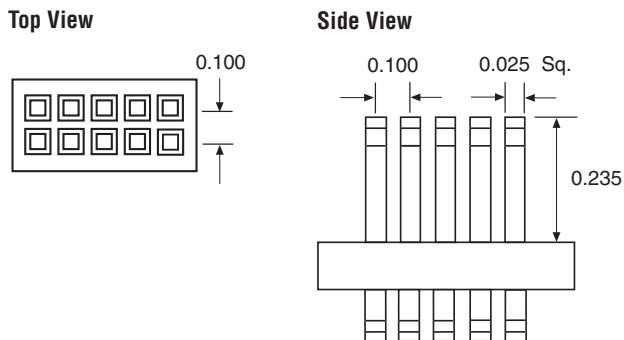
 The circuit board must supply V_{CC} and ground to the ByteBlaster II cable.

Circuit Board Header Connection

The ByteBlaster II 10-pin female plug connects to a 10-pin male header on the circuit board. The 10-pin male header has two rows of five pins, which are connected to the device's programming or configuration pins. The ByteBlaster II cable receives power and downloads data via the male header. Figure 3 shows the dimensions of a typical 10-pin male header.

Figure 3. 10-Pin Male Header Dimensions

Dimensions are shown in inches.



Operating Conditions

Tables 4 through 6 summarize the absolute maximum ratings, recommended operating conditions, and DC operating conditions for the ByteBlaster II cable.

Table 4. ByteBlaster II Cable Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground	-0.5	7.0	V
I_i	Input current		-10.0	10.0	mA
I_o	Output current		-20.0	20.0	mA

Table 5. ByteBlaster II Cable Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage, 5.0-V operation		4.5	5.5	V
	Supply voltage, 3.3-V operation		3.0	3.6	V
	Supply voltage, 2.5-V operation		2.375	2.625	V
	Supply voltage, 1.8-V operation		1.71	1.89	V

Table 6. ByteBlaster II Cable DC Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{IH}	High-level input voltage	V _{CC} = 5.5 V	2.32		V
		V _{CC} = 3.6 V	1.53		V
		V _{CC} = 2.625 V	1.11		V
		V _{CC} = 1.89 V	0.80		V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V		1.36	V
		V _{CC} = 3.0 V		0.89	V
		V _{CC} = 2.375 V		0.71	V
		V _{CC} = 1.71 V		0.51	V
V _{OH}	5.0-V high-level output voltage	V _{CC} = 4.5 V, I _{OH} = 8 mA	4.4		V
	3.3-V high-level output voltage	V _{CC} = 3.0 V, I _{OH} = 4 mA	2.9		V
	2.5-V high-level output voltage	V _{CC} = 2.375 V, I _{OH} = 2 mA	2.275		V
	1.8-V high-level output voltage	V _{CC} = 1.71 V, I _{OH} = 2 mA	1.61		V
V _{OL}	5.0-V low-level output voltage	V _{CC} = 5.5 V, I _{OL} = 8 mA		0.125	V
	3.3-V low-level output voltage	V _{CC} = 3.6 V, I _{OL} = 4 mA		0.125	V
	2.5-V low-level output voltage	TTL load. V _{CC} = 2.625 V, I _{OL} = 2 mA		0.125	
	1.8-V low-level output voltage	TTL load. V _{CC} = 1.89 V, I _{OL} = 2 mA		0.125	
I _{CC}	Operating current (No Load)			50	mA

Software Instructions

Altera's Quartus II design software package provides the programmer function required to configure or program devices using the ByteBlaster II download cable.

Quartus II Instructions

To configure or program one or more devices with the ByteBlaster II cable and the Quartus II Programmer perform the following steps.



For a detailed explanation of the programming process, see the Tutorial section of the Quartus II Help system.

1. Compile a project. The Quartus II compiler generates either an SRAM object file (.sof) file, a Programmer Object File (.pof) or a JAM STAPL format file depending on the target device.
2. Attach the ByteBlaster II cable to a parallel port on the PC running the Quartus II software and insert the 10-pin female plug into the prototype system containing the target device. The board must supply power to the ByteBlaster II cable.



A driver must be installed before using the ByteBlaster II cable with the Windows NT, Windows 2000 and Windows XP operating systems. For instructions on installing ByteBlaster II drivers, go to the “ByteBlaster II and MasterBlaster Installation” section in the *Quartus II Installation and Licensing for PCs Manual*.

3. Open the Quartus II programmer by selecting **Programmer** from the (Tools menu). Choose **Setup** in the Programming Hardware section. Specify the ByteBlaster II cable and the appropriate LPT port. Please see “Changing Setup” under the ByteBlaster II cable in the Quartus II software Help menu for more information.
4. Select either active serial, passive serial, or JTAG programming mode and then add the files and/or devices you want to program or configure using the **add file** or **add device** buttons to create a chain description file (.cdf).

The programmer has three programming modes: active serial, passive serial, and JTAG. In active serial mode, a single EPCS POF is selected, and you can choose from several programming options. In passive serial mode, you select which SOFs to include in the device chain. In JTAG mode, you add specific devices and configuration devices to the device chain, in addition to POFs and SOFs, and you have several programming options for each configuration device in the chain.

In JTAG mode, you can verify EPC configuration device contents against its programming file data, check that a device is blank, examine a programmed device and save its data to file, or use its data to program or verify another configuration device. You can perform these functions for EPCS configuration devices using active serial mode.

5. Click **start** in the Quartus II Programmer to program or configure the device(s). The ByteBlaster II cable downloads the data from the SOF and/or POF file(s) into the device(s).



For further information, refer to the tutorial section of the Quartus II Help. (Contact Altera for support if using the MAX+PLUS II® software.)

Conclusion

Downloading configuration and programming data directly to the device via the ByteBlaster II cable allows designers to verify multiple design iterations in quick succession, thereby speeding the design cycle.

References

For more information on configuration and in-system programmability (ISP), see the following sources:

- *AN 39: IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*
- *AN 95: In-System Programmability in MAX Devices*
- *AN 116: Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices*
- *AN 208: Configuring Stratix & Stratix GX Devices*
- *AN 250: Configuring Cyclone FPGAs*
- *Serial Configuration Devices Data Sheet*
- Search for "ByteBlaster II," "Programming a Single Device or Multiple Devices in JTAG or Passive Serial Chains with the MasterBlaster or ByteBlaster II", "Configuration Scheme Description", "Programmer Introduction," and "Programming" in the Quartus II Help system.



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