MS7318M1 Version: 100

CPU:

Intel LGA775
(Support Conroe E6300/E6400/E6700/E6800,
Prescott 500 Sequence, Cedar Mill,
Smithfield, Celeron D)

System Chipset:

VIA PT890CE (North Bridge)
VIA VT8251L (South Bridge)

On Board Chipset:

CLOCK - ICS953002 + ICS9P936
LPC Super I/O - W83627DHG
BIOS - LPC ROM
HD Audio ALC888
LAN - Realtek 8201CL colay RT8110SC
IEEE1394 - VT6308P
E-SATA JMB360

Main Memory:

single-channel - DDRII*2 533

Expansion Slots:

PCI Express X16 * 1
PCI 2.3 Slot * 1 (Medion 2 master)
PCI 2.3 Slot * 1
PCI Express X1 * 1

PWM VRD11 :

Intersil 6312 3 Phase

MSI MICRO-START INT'L CO.,LTD.

Title	Cover Sheet	
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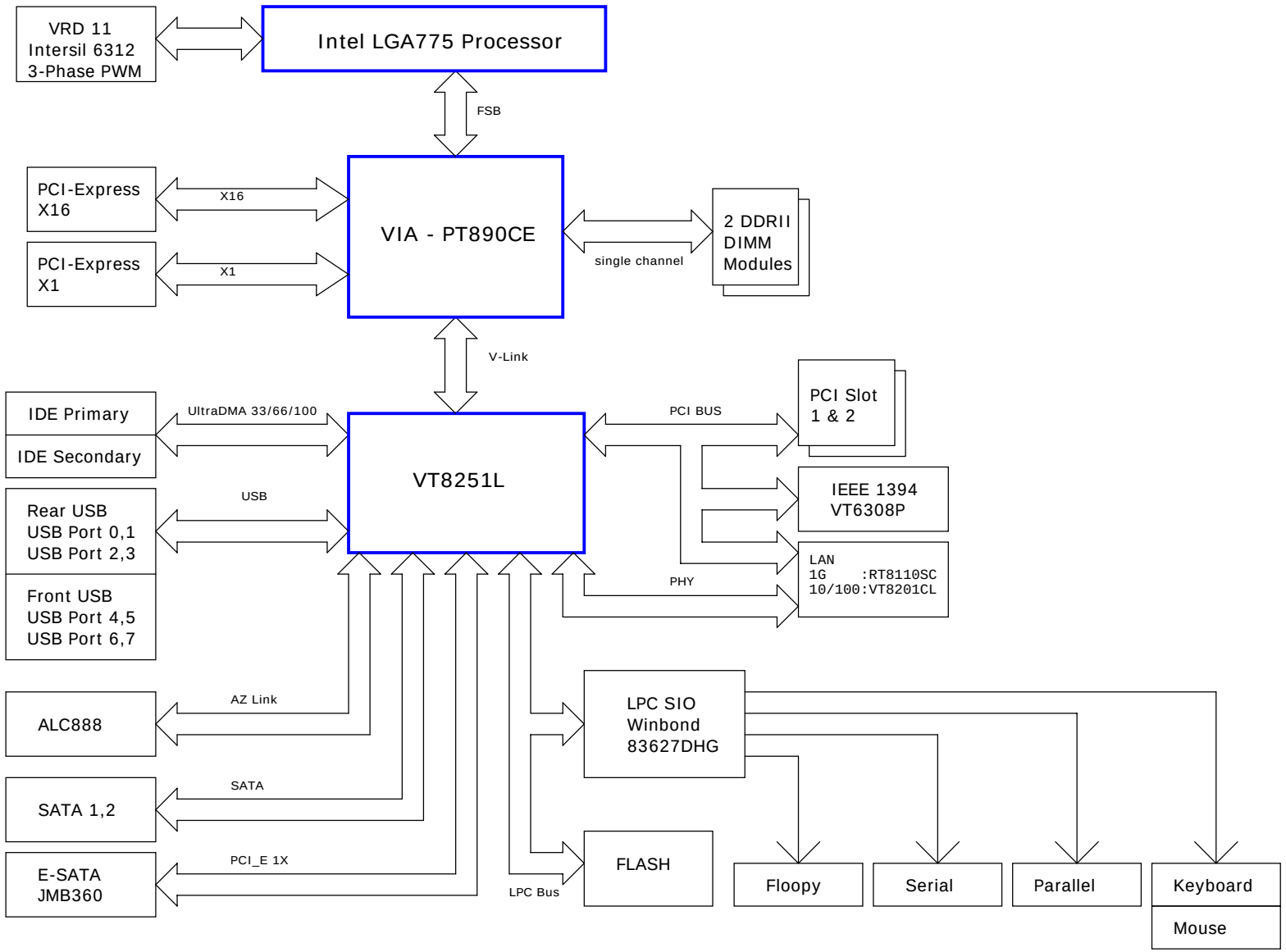
Block Diagram



MICRO-START INT'L CO.,LTD.

Title	Block Diagram	
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System Chipset General Purpose I/O

Name	Pin	Type	Function Description	Normal	Activ
GPI0	AB04	I	Pull High to VBAT	High	
GPI1	AB02	I	Not Used; Pull High Only	High	
GPI2/EXTSMI#	W02	I	EXTSMI#(Medios Funtion)	High	Low
GPI3/RING#	Y03	I	RING#	High	Low
GPI4/LID#	AA02	I	HM_SMI#	High	Low
GPI5/BATLOW#	Y01	I	Not Used; Pull High Only	High	
GPI6/ASPBZ#	AF06	I	ASPBZ#		
GPI7/REQ5#	L01	I	Not Used; Pull High Only	High	
GPI8	A28	I	No Used; Pull Low Only	High	
GPI16/REQ6#	M01	I	Not Used; Pull High Only	High	
GPI17/CPUMISS/SACSDIN	U04	I	ATADET0, Low 80 pin cable		
GPI18/THRM#/ADLGPI	W03	I	PEPMESCI#	VSUS33	
GPI19/APICCLK	AB26	I	APICCLK		
GPI20/ACSDIN2/PCS0#	T03	I	ACSDIN2		
GPI21/ACSDIN3/PCS1#	T01	I	ACSDIN3		
GPI22/SAGP1	AE08	I	Not Used; NC		
GPI23/SAGP2	AF07	I	Not Used; NC		
GPI28/SAGP3	AG07	I	Not Used; NC		
GPI29/SAGP4	AF08	I	Not Used; NC		
GPI32/INTE#	P04	I	Not Used; Pull High Only	High	
GPI33/INTF#	N04	I	Not Used; Pull High Only	High	
GPI34/INTG#	N01	I	Not Used; Pull High Only	High	
GPI35/INTH#	N02	I	INTH#		
GPI36/USBOC4#	B25	I	USBOC4#	High	Low
GPI37/USBOC5#	A25	I	USBOC5#	High	Low
GPI38/USBOC6#	A26	I	USBOC6#	High	Low
GPI39/USBOC7#	D25	I	USBOC7#	High	Low
GPO0	W04	O	EN_PCIERST	VSUS33	
GPO1	AC01	O	Not Used; Pull High Only	High	
GPO2/SUSA#	W01	O	Not Used; Pull High Only	High	
GPO3/SUSST#	Y02	O	SUSST#	High	Low
GPO4/SUSCLK	Y01	O	SUSCLK		
GPO5/CPUSTP#	AD05	O	Not Used; Pull High Only	High	
GPO6/PCISTP#	AD04	O	Not Used; Pull High Only	High	
GPO7/GNT5#	M04	O	GNT5#		
GPO8/GPIB/VGATE	AG06	O	Not Used; Pull High Only	High	
GPO9	C27	O	Not Used; Pull Low Only		
GPO20/GNT6#	N03	OD	GNT6#		
GPO21/ACSDOUT1/SACSD	T02	OD	ACSDOUT1	VCC33	
GPO22/GHI#	W28	OD	Not Used; Pull High Only	High	
GPO23/OPSLP#	Y28	OD	Not Used; Pull High Only	High	
GPO28/VIDSEL	AH06	OD	Not Used; Pull High Only	High	
GPO29/VRDSLP	AE07	OD	Not Used; Pull High Only	High	
GPI10/GPO10/APICD0	W25	IO	Not Used; Pull High Only	VCC33	
GPI011/APICD1	W26	IO	Not Used; Pull High Only	VCC33	
GPI012/GPIOE/SACRST#	AH02	IO	Not Used; NC	VSUS33	
GPI013/GPIOF/SACBITCL	AG03	IO	Not Used; NC	VSUS33	
GPI014/GPIOG/SACSYNC	AH03	IO	Not Used; NC	VSUS33	
GPI015/GPIOH	AF04	IO	Not Used; NC	VSUS33	
GPI024/GPIOA/PEREQA	AE03	IO	Not Used; Pull High Only	VCC33	
GPI025/GPIOB/PEREQB	AE01	IO	Not Used; Pull Low Only	VCC33	
GPI026/SMBDT2	AB03	IO	SMBDT2	VSUS33	
GPI027/SMBCK2	Y04	IO	SMBCK2	VSUS33	
GPI030/GPIOC/PCSNTA	AF03	IO	Not Used; Pull High Only	VCC33	
GPI031/GPIOD/PCSNTB	AC05	IO	Not Used; Pull Low Only	VCC33	

Super I/O General Purpose I/O Super I/O default clock frequency is 48MHz

Name	Pin	Function Description	Normal	Activ
GP10 / GPSA1	128	N/A		
GP11 / GPSB1	127	N/A		
GP12 / GPX1	126	N/A		
GP13 / GPX2	125	N/A		
GP14 / GPY2	124	N/A		
GP15 / GPY1	123	N/A		
GP16 / GPSB2	122	N/A		
GP17 / GPSA2	121	N/A		
GP20 / CPUFANOUT1	120	NC		
GP21 / CPUFANIN1	119	NC		
GP22 / SCE#	19	NC		
GP23 / SCK	2	33MHz clock output for Debug		
GP24 / MDAT#	66	MSDAT#		
GP25 / MCLK#	65	MSCLK#		
GP26 / KDAT#	63	KBDAT#		
GP27 / KCLK#	62	KB CLK#		
GP30	92	NC		
GP31	91	CPU_FAN_TYPE		
GP32 / PSTOUT2#	90	NC		
GP33 / PSTOUT3#	89	NC		
GP34 / RSTOUT4#	88	NC		
GP35	87	NC		
GP36	69	NC		
GP37	64	NC		
GP40 / RIB#	85	RIB#		
GP41 / DCDB#	84	DCDB#		
GP42 / IRTX / SOUTB	83	SOUTB_IRTX		
GP43 / IRRX / SINB	82	SINB_IRRX		
GP44 / DTRB#	81	DTRB#		
GP45 / RTSB#	80	DTSB#		
GP46 / DSRB#	79	DSRB#		
GP47 / CTSB#	78	CTSB#		
GP50 / EN_GTL / WDTO#	77	EN_GTL		
GP51 / RSMRST#	75	NC		
GP52 / SUSB#	73	SLP_S3#		
GP53 / PSON#	72	PS_ON#(5VSB)		
GP54 / PGROK	71	PWROK		
GP55 / SUSLED	70	NC		
GP56 / PSIN	68	PS_IN#		
GP57 / PSOUT	67	PWRBTN#		
GP60 / RIA#	57	RIA#		
GP61 / DCDA#	56	DCDA#		
GP62 / PENKBC / SOUTA	54	SOUTA		
GP63 / SINA	53	SINA		
GP64 / PENROM / DTRA#	52	DTRA#		
GP65 / HEFRAS / RTSA#	51	RTSA#		
GP66 / DSRA#	50	DSRA#		
GP67 / CTSA#	49	CTSA#		

PCI Config.

DEVICE	MCP1 INT Pin	REQ# /GNT#	IDSEL	CLOCK	CLK GEN Pin Out
PCI Slot 1	**PIRQ#A** PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD20	CK_PCI_CLK0	11
	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD21	CK_PCI_CLK1	14
PCI Slot 2	**PIRQ#C** PIRQ#D PIRQ#A PIRQ#B	PREQ#2 PGNT#2	AD22	CK_PCI_CLK2	17
1394	**PIRQ#D**	PREQ#3 PGNT#3	AD23	1394_PCLK	13
LAN	**PIRQ#A**	PREQ#4 PGNT#4	AD24	PCI_CLK_LAN	13

PIRQ#A also link to NB PIN H13
PIRQ#H also link to NB PIN B6

PCI RESET DEVICE

Signals	Source	Target
PCIRST#	VT8237A	MS7
PCIRST#1	MS7	1394 & SPIO & BIOS
PCIRST#2	MS7	PCI slot 1-2
NB_RST#	MS7	NB_RST#
HDRST#	MS7	Primary, Scondary IDE
Rsmrst#	MS7	VT8237A
PCIE_Reset#	VT8237A	PCIE 1-2

DDR DIMM Config.

RAMTYPE	2 DDR DIMM
DIMM 1 Slave	1010 0000 (A0)
DIMM 2 Slave	1010 0010 (A2)

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Title: GPIO/Memory/PCI/HW Config.

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SB-VT5251LCE

Strap Pins			
(External pullup / pulldown straps are required to select “H” / “L”)			
Strap Pins for VT8251L Version CE Configuration			
Signal	Pin#	Function	Description
SPKR	AF05	CPU Frequency Strapping	L: Enable CPU Frequency Strapping H: Disable CPU Frequency Strapping Default setting: Disable
ACSDOUT0	R01	Auto Reboot	L: Enable Auto Reboot H: Disable Auto Reboot . Default setting: Disable
SEEDI	B13	Use Serial External LAN EEPROM	L: Enable. Use external EEPROM H: Disable. Do not use external EEPROM Default setting: Enable (pull low) sInc
ACSYNC	R04	LPC FWH	L: Enable LPC FWH Command H: Disable LPC FWH Command **Default setting: Disable**
PDCS1#	AC25	SATA Spin Up Mode Vlink auto compensation	L: Enable SATA spin up mode iel H: Disable SATA spin up mode Default setting: Disable
PDDACK#	AB23	PCI Express Debugging Mode	L: Enable PCI Express debugging mode logntiaired H: Disable PCI Express debugging mode Default setting: Disable
SUSA#	W01	Notebook / Desktop LAN Reset	L: Notebook LAN reset H: Desktop LAN reset hnoideequ
Strap Pins for North Bridge (“NB”) Configuration			
PDCS3#	AA23	NB Configuration ATeCon	PDCS3# signal state is reflected on signal pin VD7 during power up for North Bridge configuration.
PDA2	AD27	NB Configuration	PDA2 signal state is reflected on signal pin VD6 during power up for North Bridge configuration.
PDA1	AC26	NB Configuration	PDA1 signal state is reflected on signal pin VD5 during power up for North Bridge configuration. DAR
GPIOD / PCGNTB	AC05	NB Configuration	NGPIOD/PCGNTB signal state is reflected on signal pin VD3 during power up for North Bridge configuration.
GPIOB / PCREQB	AE01	NB Configuration	GPIOB/PCREQB signal state is reflected on signal pin VD2 during power up for North Bridge configuration.
PDA0, GPIOA/PCREQA GPIOC/PCGNTA	AE03 AF03	NB Configuration	PDA0, GPIOA/PCREQA and GPIOC/PCGNTA signal states are reflected on signal pins VD4, VD1 and VD0 during power up for North Bridge configuration.

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Title	Strap Pins	
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Ce = 2 CL - Ci - Cs
= (2 x 32) - 5 - 3
= 56

U8

ICS953002DFLF-T_SSOP56-RH

Ver : D

SEL24_48

1=24MHz , 0=48MHz

MODE

0 = DESKTOP MODE

CLOCK STRAPPING

BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	267 MHZ (1067)
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)

U23

ICS9P936AFLF_SSOP28-LF

RN50

8P4R-10R0402

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Title: CLOCK GEN & BUFFER

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CPU SIGNAL BLOCK

CPU1A

ZIF-SOCK775-15u

15 // 10 / 10 / 10 //15

FSBSEL RESISTOR CAN BE REMOVED IF ONLY TEJAS
AND CEDAR MILL ARE SUPPORTED

N12-7750020-A10

AP339E

VID PULL-HI

FOR DUAL CORE CPU

Prescott / Cedar Mill
LL_ID[1:0] = 00
GTLREF_SEL = 0
VTT_SEL = 1

PLACE BPM TERMINATION NEAR CPU

BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	267 MHZ (1067)
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)

Micro Star Restricted Secret

Title	Intel LGA775 - Signals
Rev	100
Document Number	MS-7318-0B-060828E

MICRO-STAR INT'L CO., LTD.
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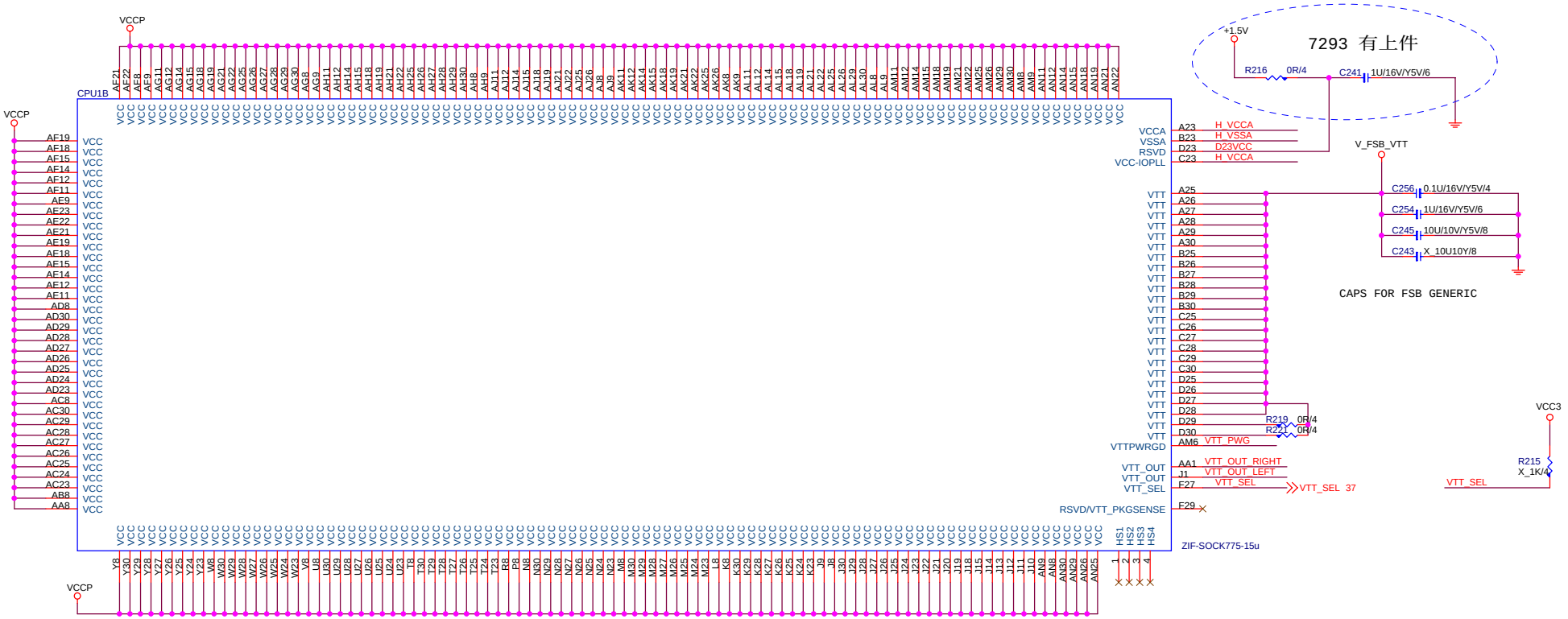

Micro Star Restricted Secret

Title	Intel LGA775 - Power
Rev	100
Document Number	MS-7318-0B-060828E

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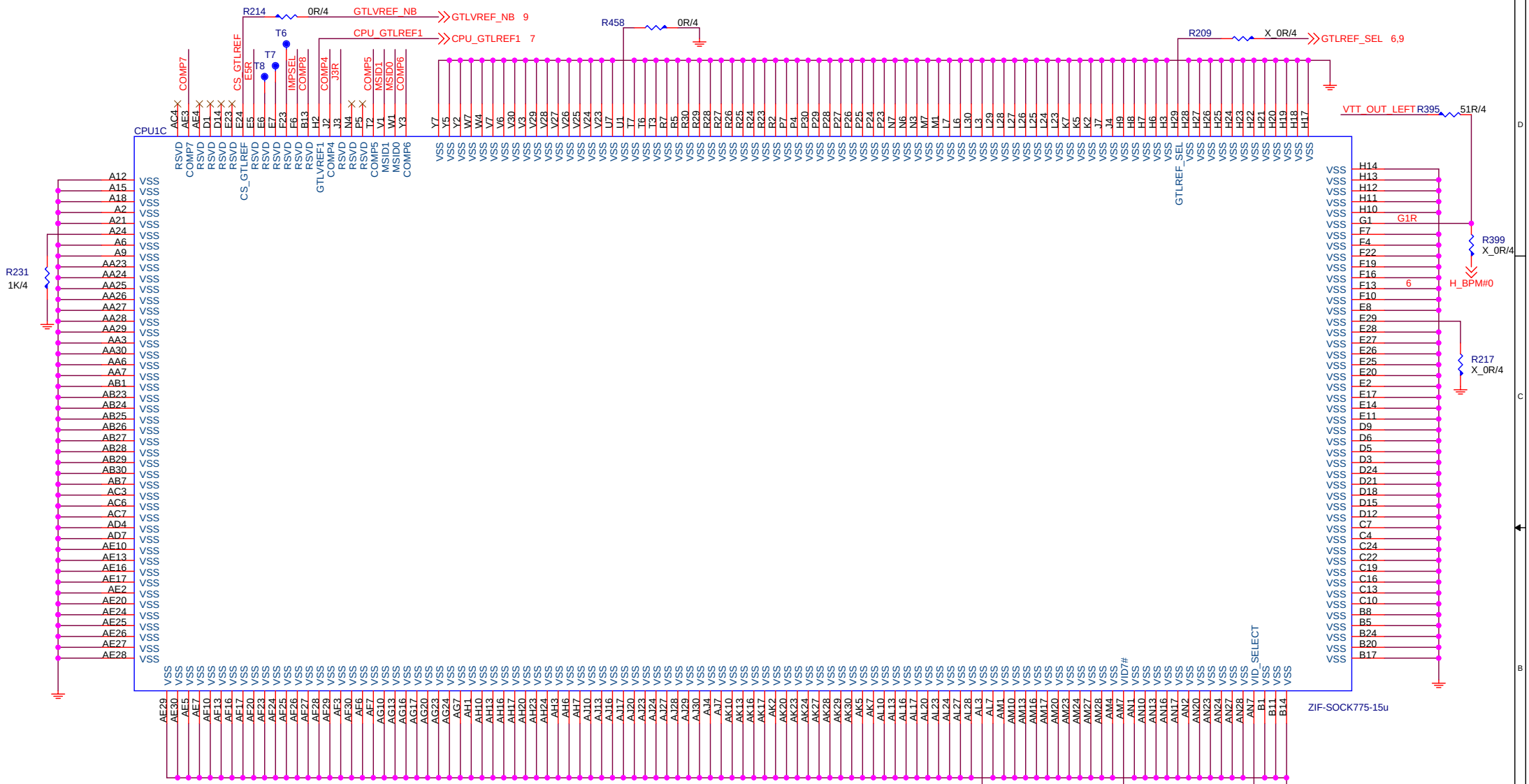

	MSID1	MSID0
2005 Perf FMB	0	0
2005 Value FMB	0	1 / NC

Micro Star Restricted Secret

Title	Intel LGA775- GND
Rev	100
Document Number	MS-7318-0B-060828E
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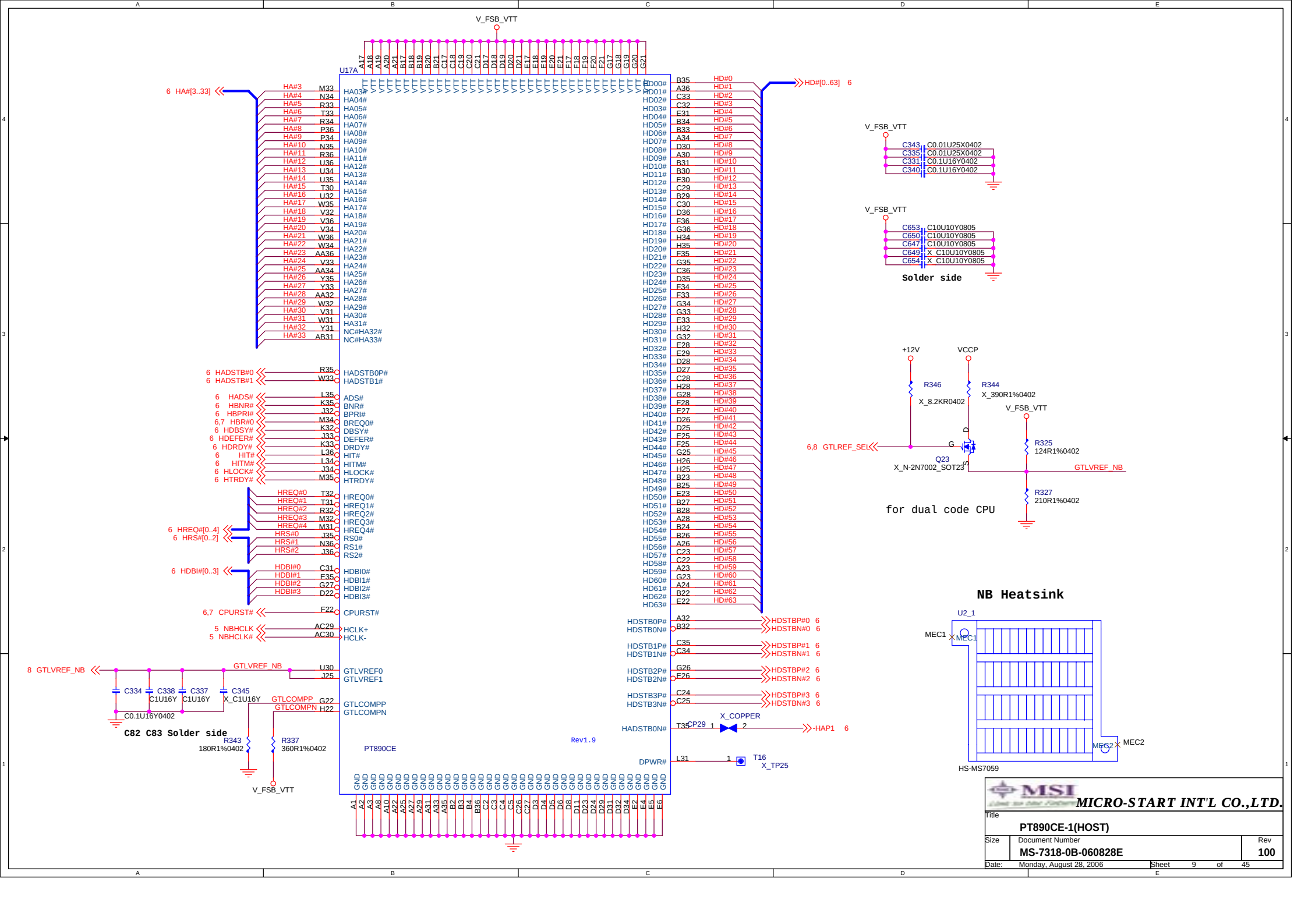

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Title	PT890CE-1(HOST)	
Size	Document Number: MS-7318-0B-060828E	Rev: 100
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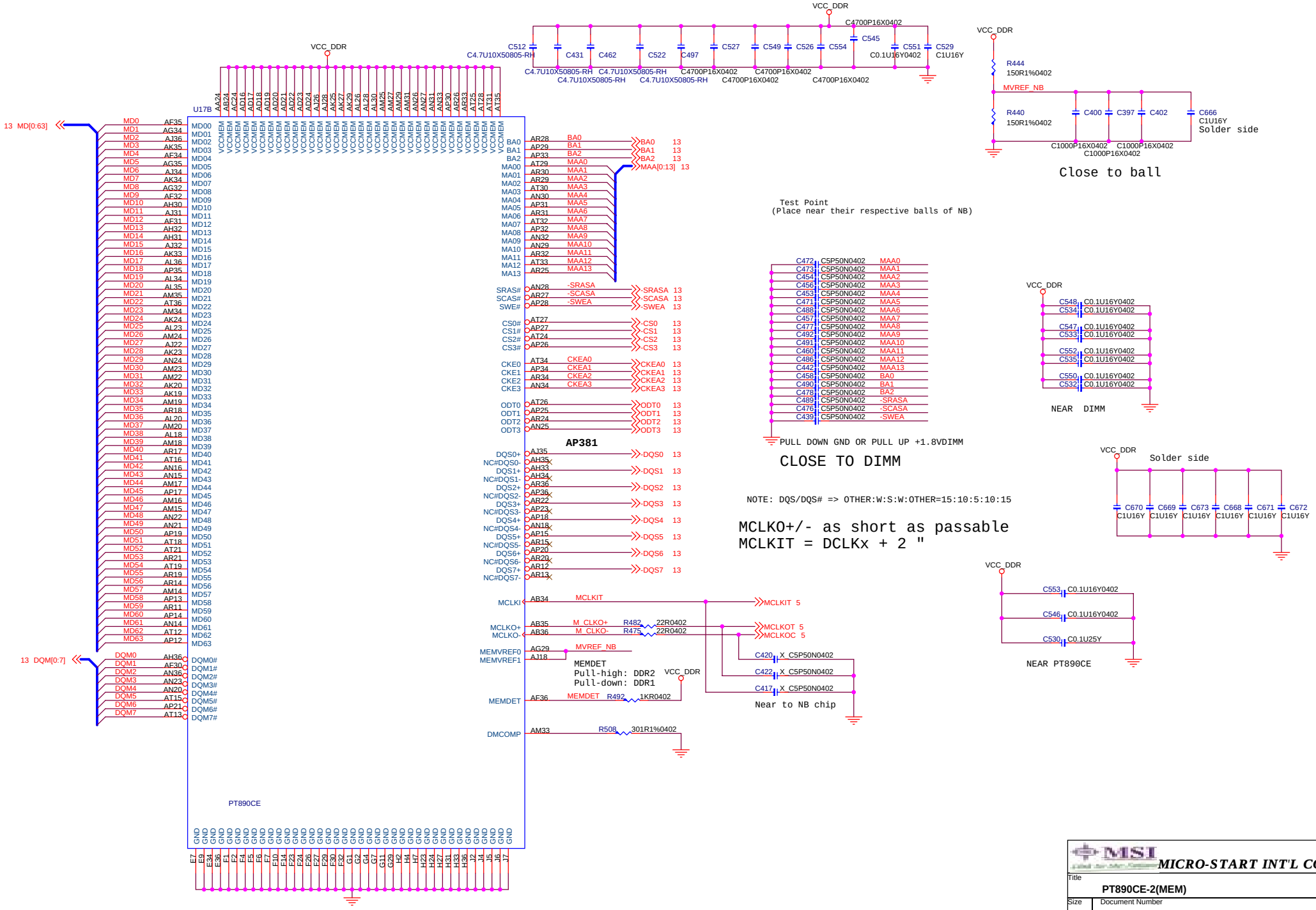
VCC_DDR
C4700P16X0402
C512 C4.7U10X50805-RH
C431 C4.7U10X50805-RH
C462 C4.7U10X50805-RH
C522 C4.7U10X50805-RH
C497 C4700P16X0402
C527 C4700P16X0402
C549 C4700P16X0402
C526 C4700P16X0402
C554 C4700P16X0402
C545
C551 C0.1U16Y0402
C529 C1U16Y
R444 150R1%0402
MVREF_NB
R440 150R1%0402
C400 C1000P16X0402
C397 C1000P16X0402
C402 C1000P16X0402
C666 C1U16Y Solder side
Close to ball
U17B
PT890CE
13 MD[0:63]
13 DQM[0:7]
Test Point
(Place near their respective balls of NB)
PULL DOWN GND OR PULL UP +1.8VDIMM
CLOSE TO DIMM
NEAR DIMM
Solder side
NOTE: DQS/DQS# => OTHER:W:S:W:OTHER=15:10:5:10:15
MCLKO+/- as short as passable
MCLKIT = DCLKx + 2 "
AP381
MEMDET
Pull-high: DDR2
Pull-down: DDR1
Near to NB chip
NEAR PT890CE
MICRO-START INT'L CO.,LTD.
Title
PT890CE-2(MEM)
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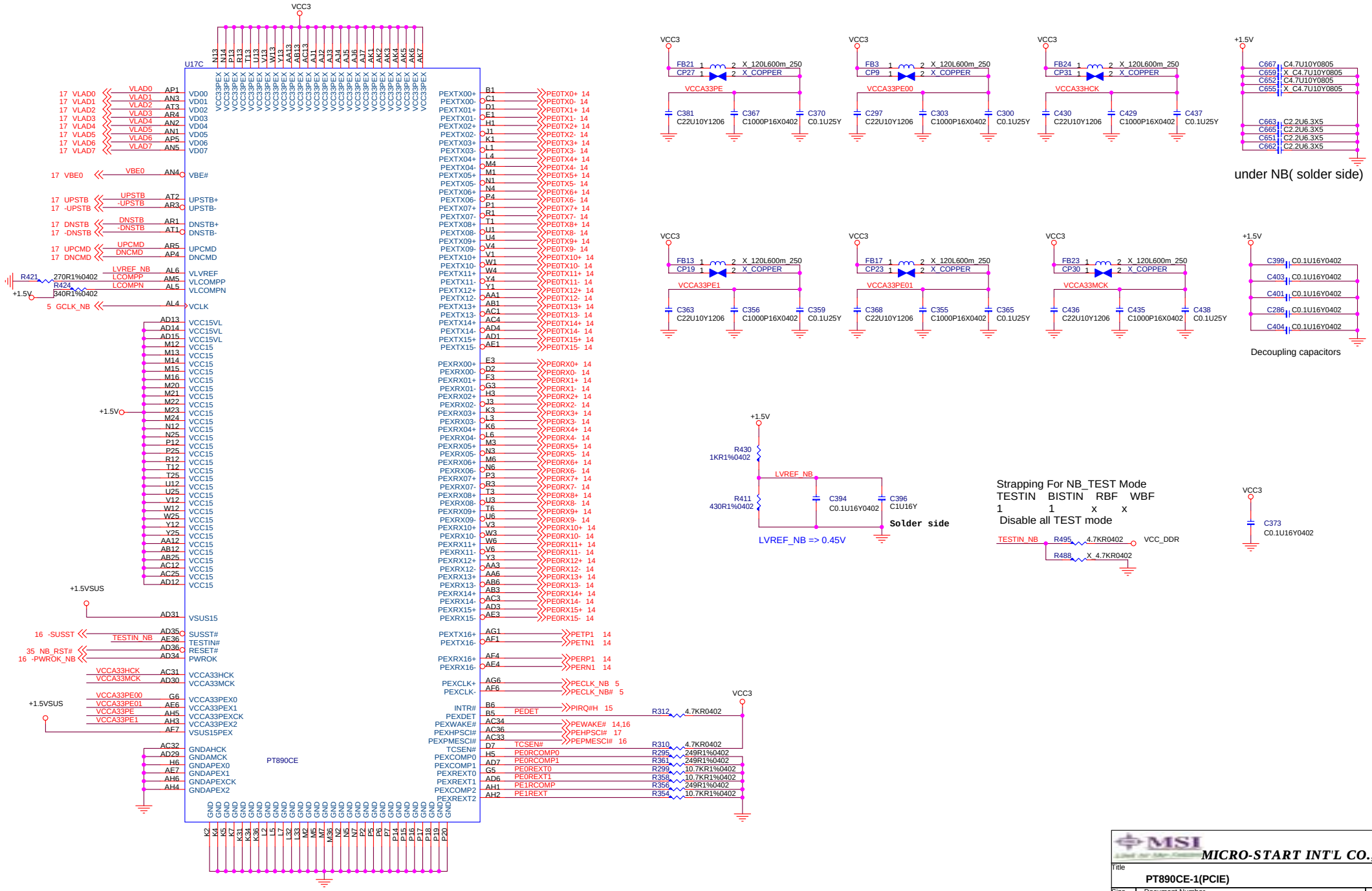

MICRO-START INT'L CO.,LTD.

Title	PT890CE-1(PCIE)	
Size	Document Number: MS-7318-0B-060828E	Rev: 100
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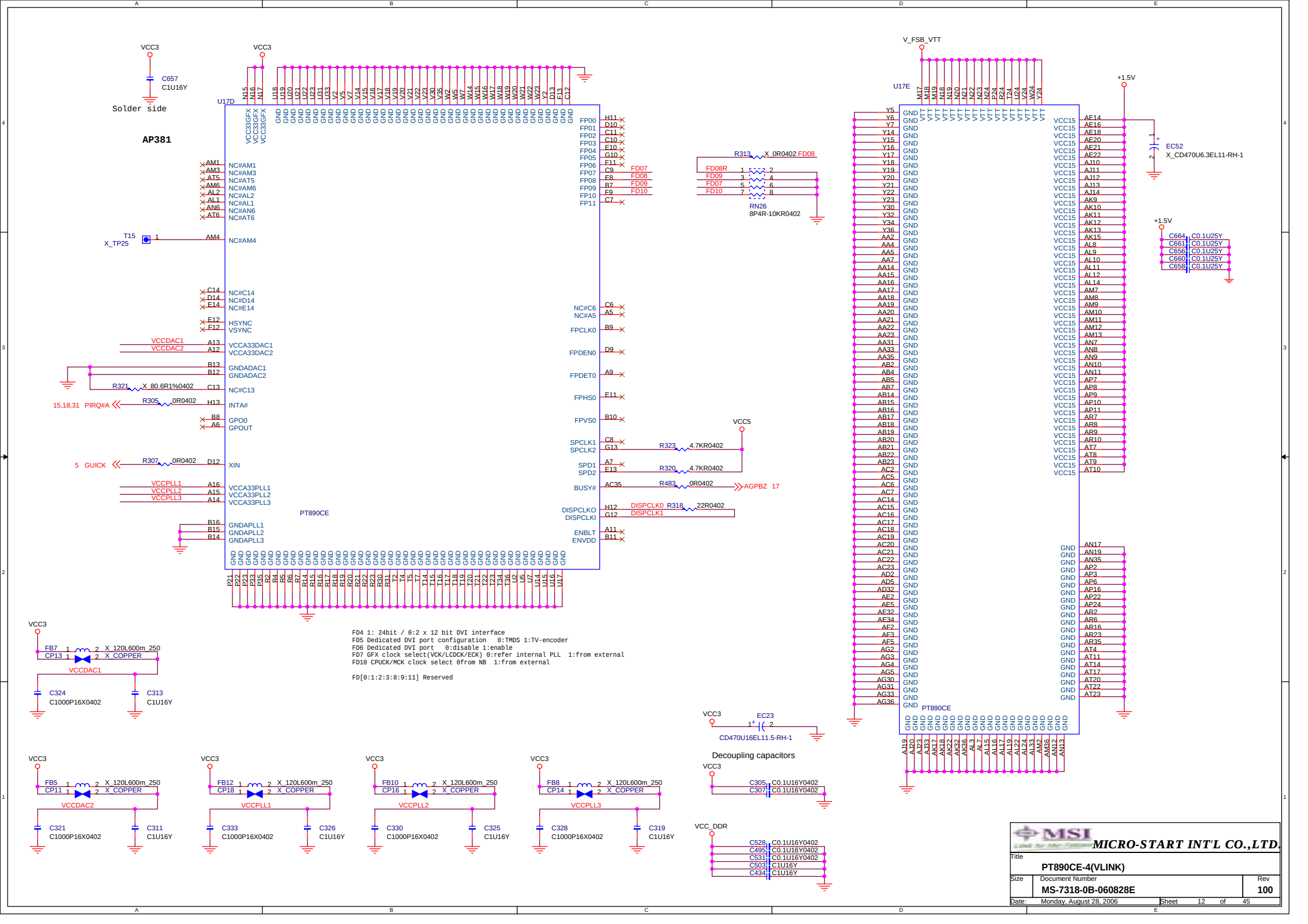
VCC3
C657
C1U16Y
Solder side
AP381
U17D
PT890CE
NC#AM1
NC#AM3
NC#AT5
NC#AM6
NC#AL2
NC#AL1
NC#AN6
NC#AT6
NC#AM4
NC#C14
NC#D14
NC#E14
HSYNC
VSYNC
VCCA33DAC1
VCCA33DAC2
GNDADAC1
GNDADAC2
NC#C13
INTA#
GPO0
GPOUT
XIN
VCCA33PLL1
VCCA33PLL2
VCCA33PLL3
GNDAPLL1
GNDAPLL2
GNDAPLL3
FPD00
FPD01
FPD02
FPD03
FPD04
FPD05
FPD06
FPD07
FPD08
FPD09
FPD10
FPD11
NC#C6
NC#A5
FPCLK0
FPDEN0
FPDET0
FPHS0
FPVS0
SPCLK1
SPCLK2
SPD1
SPD2
BUSY#
DISPCLKO
DISPCLKI
ENBLT
ENVDD
R313 X_0R0402 FD08
RN26
8P4R-10KR0402
R321 X_80.6R1%0402
R305 0R0402
15,18,31 PIRQ#A
5 GUICK
R307 0R0402
R323 4.7KR0402
R320 4.7KR0402
R483 0R0402
AGPBZ 17
R318 22R0402
DISPCLK0
DISPCLK1
VCC5
FD4 1: 24bit / 0:2 x 12 bit DVI interface
FD5 Dedicated DVI port configuration 0:TMDS 1:TV-encoder
FD6 Dedicated DVI port 0:disable 1:enable
FD7 GFX clock select(VCK/LCDCK/ECK) 0:refer internal PLL 1:from external
FD10 CPUCK/MCK clock select 0from NB 1:from external
FD[0:1:2:3:8:9:11] Reserved
FB7 X_120L600m_250
CP13 X_COPPER
VCCDAC1
C324 C1000P16X0402
C313 C1U16Y
FB5 X_120L600m_250
CP11 X_COPPER
VCCDAC2
C321 C1000P16X0402
C311 C1U16Y
FB12 X_120L600m_250
CP18 X_COPPER
VCCPLL1
C333 C1000P16X0402
C326 C1U16Y
FB10 X_120L600m_250
CP16 X_COPPER
VCCPLL2
C330 C1000P16X0402
C325 C1U16Y
FB8 X_120L600m_250
CP14 X_COPPER
VCCPLL3
C328 C1000P16X0402
C319 C1U16Y
V_FSB_VTT
U17E
PT890CE
+1.5V
EC52
X_CD470U6.3EL11-RH-1
C664 C0.1U25Y
C661 C0.1U25Y
C656 C0.1U25Y
C660 C0.1U25Y
C658 C0.1U25Y
EC23
CD470U16EL11.5-RH-1
Decoupling capacitors
C305 C0.1U16Y0402
C307 C0.1U16Y0402
VCC_DDR
C528 C0.1U16Y0402
C495 C0.1U16Y0402
C531 C0.1U16Y0402
C503 C1U16Y
C434 C1U16Y
MICRO-START INT'L CO.,LTD.
Title
PT890CE-4(VLINK)
Size
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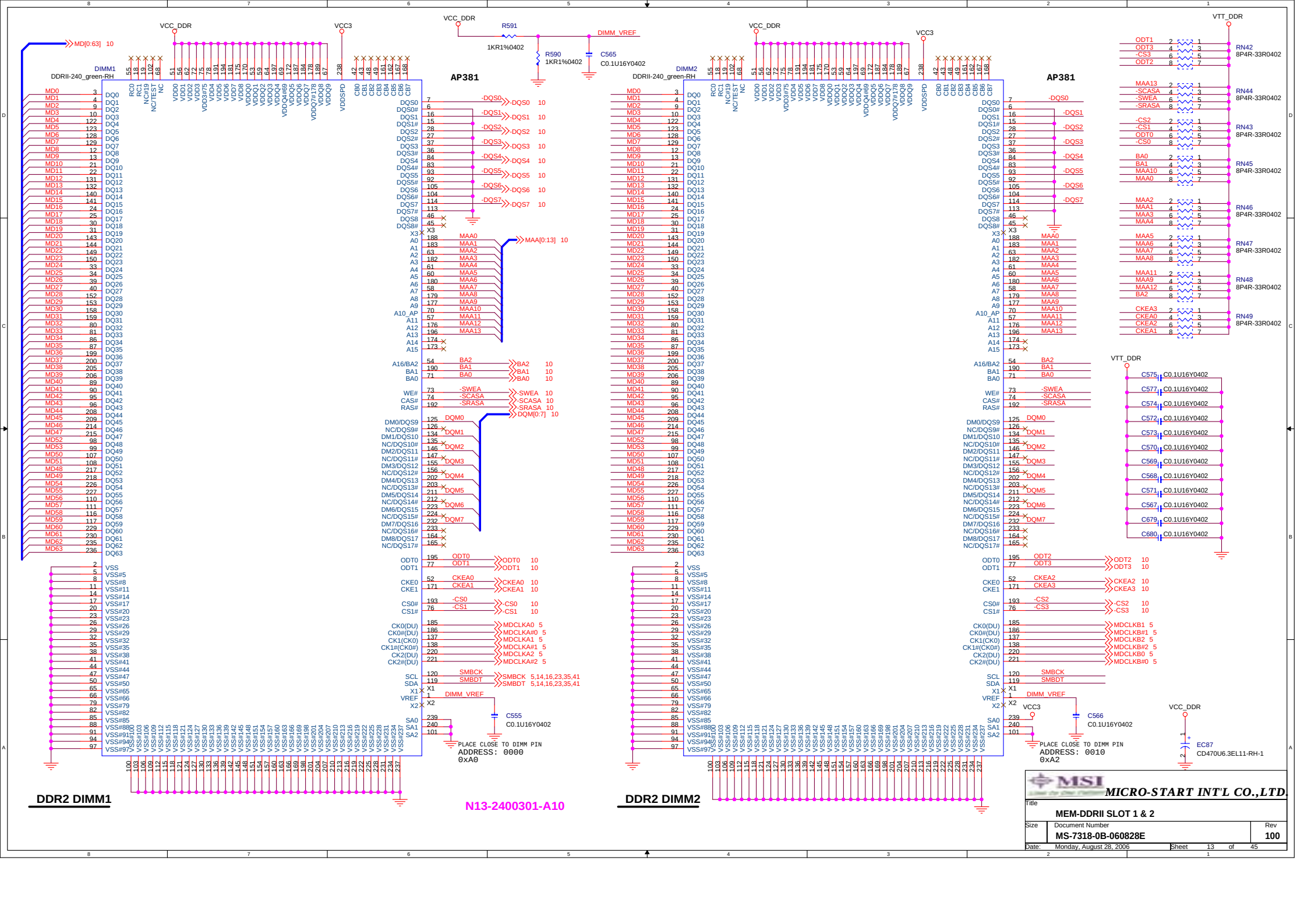
DDR2 DIMM1
DDR2 DIMM2
DIMM1
DIMM2
DDRII-240_green-RH
AP381
VCC_DDR
VCC3
VTT_DDR
R591
1KR1%0402
R590
1KR1%0402
DIMM_VREF
C565
C0.1U16Y0402
C555
C0.1U16Y0402
C566
C0.1U16Y0402
EC87
CD470U6.3EL11-RH-1
MD[0:63] 10
MAA[0:13] 10
DQM[0:7] 10
PLACE CLOSE TO DIMM PIN
ADDRESS: 0000
0xA0
ADDRESS: 0010
0xA2
N13-2400301-A10
MICRO-START INT'L CO.,LTD.
MEM-DDRII SLOT 1 & 2
MS-7318-0B-060828E
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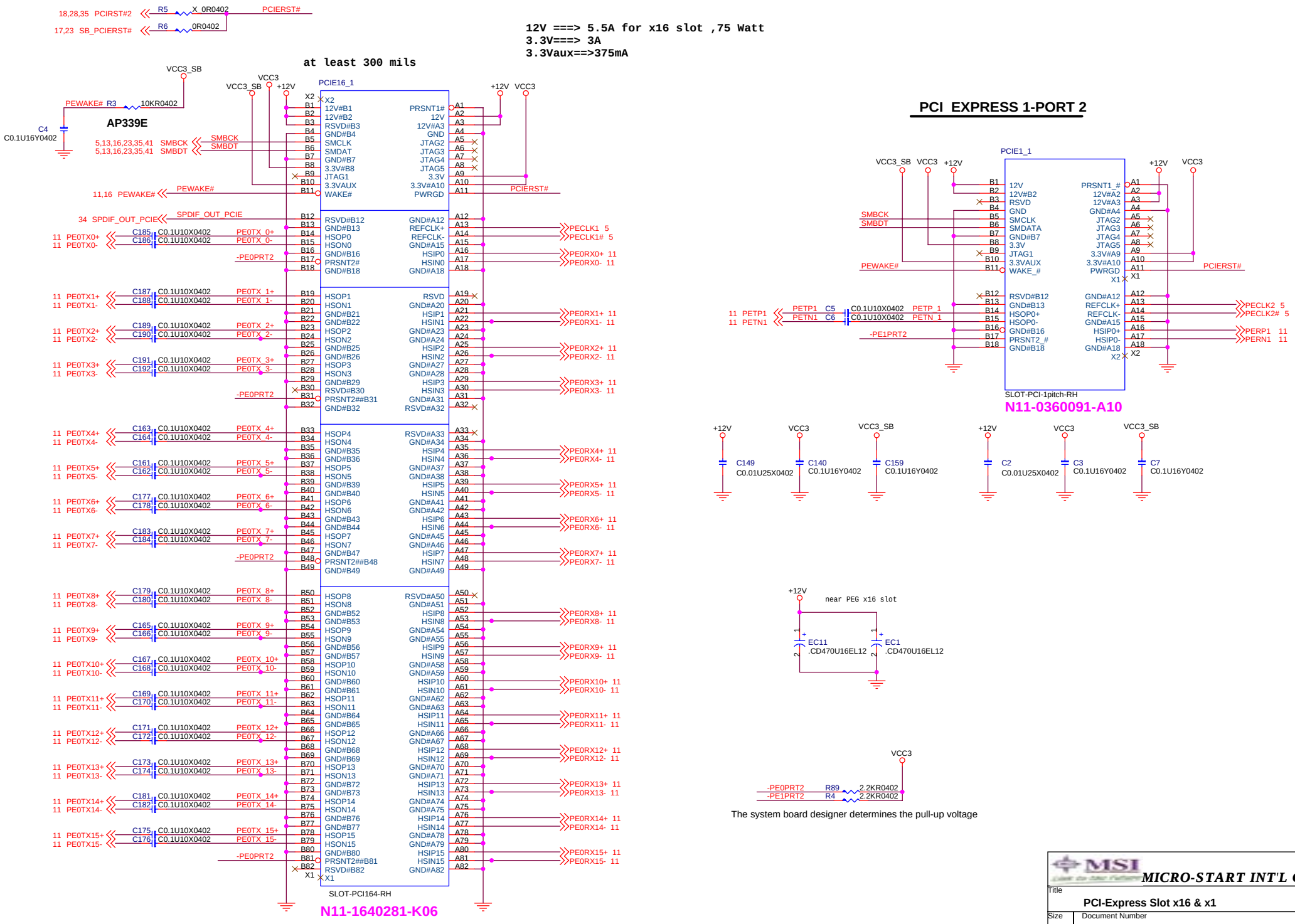
12V ===> 5.5A for x16 slot ,75 Watt
3.3V===> 3A
3.3Vaux==>375mA
at least 300 mils
AP339E
PCIE16_1
SLOT-PCI164-RH
N11-1640281-K06
PCI EXPRESS 1-PORT 2
PCIE1_1
SLOT-PCI-1pitch-RH
N11-0360091-A10
near PEG x16 slot
The system board designer determines the pull-up voltage
MICRO-START INT'L CO.,LTD.
PCI-Express Slot x16 & x1
MS-7318-0B-060828E
100
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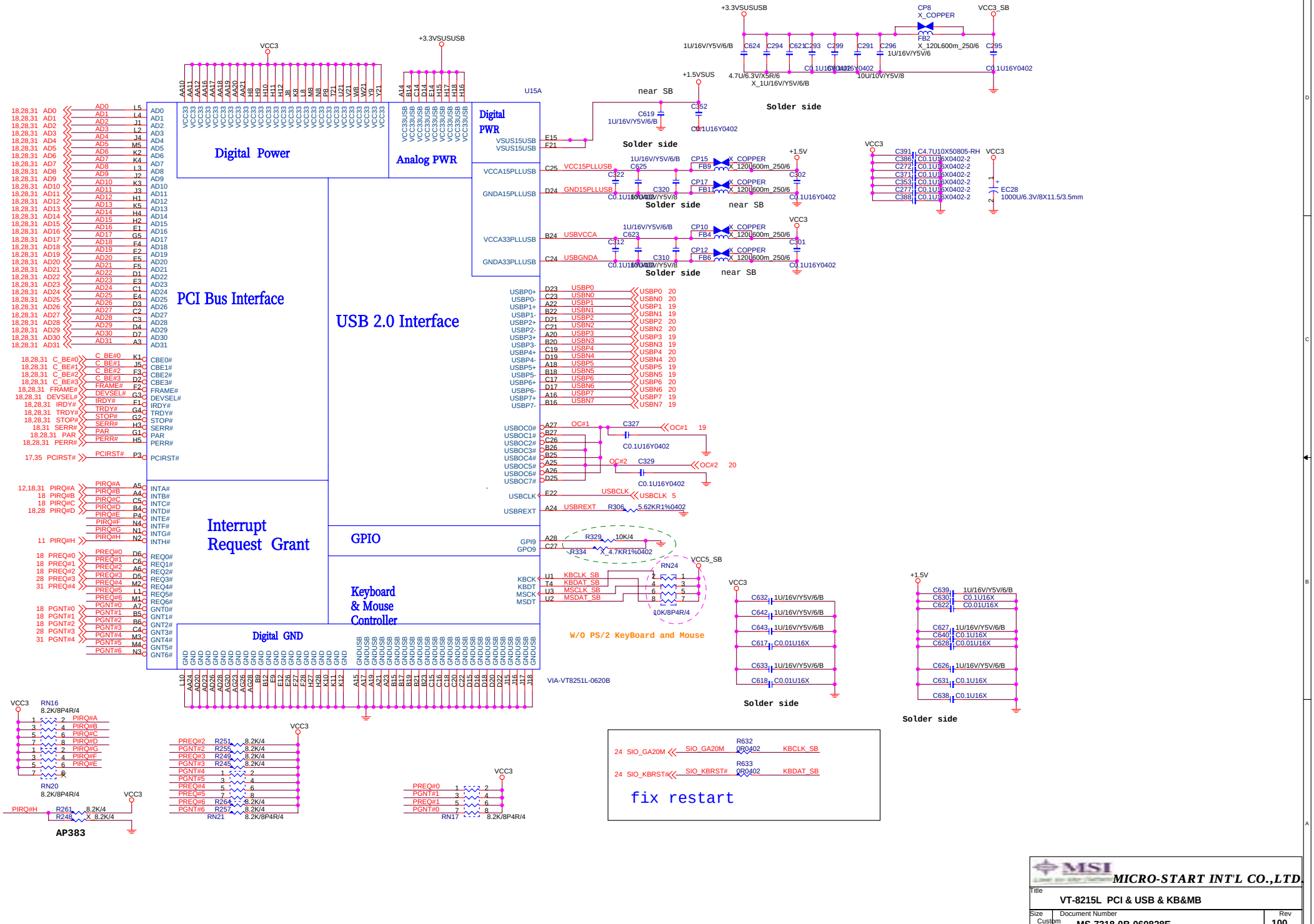
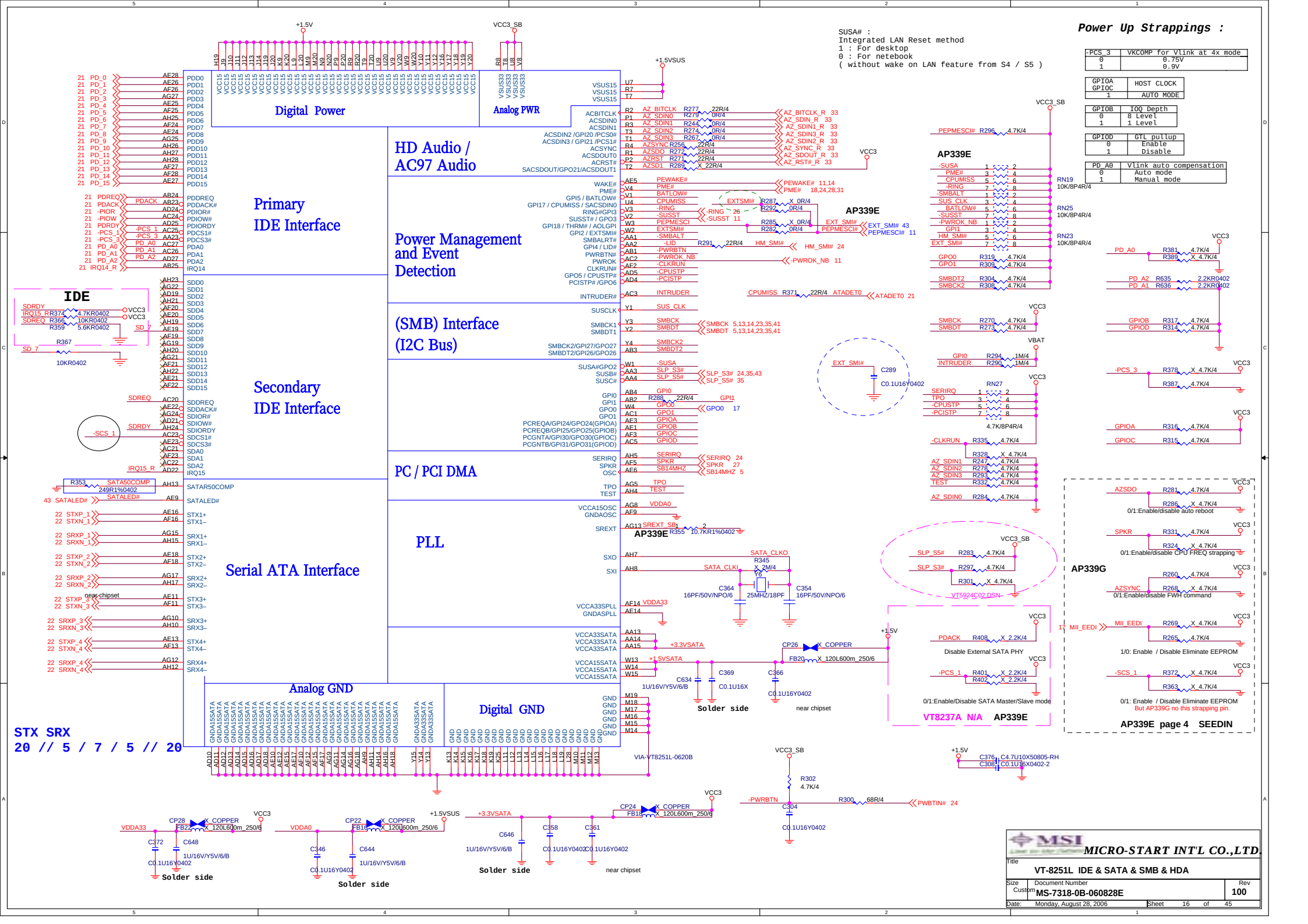

Digital Power
Analog PWR
PCI Bus Interface
USB 2.0 Interface
Interrupt Request Grant
GPIO
Keyboard & Mouse Controller
Digital GND
VIA-VT8251L-0620B
W/O PS/2 KeyBoard and Mouse
Solder side
near SB
AP383
fix restart
MICRO-START INT'L CO.,LTD.
VT-8215L PCI & USB & KB&MB
MS-7318-0B-060828E
Monday, August 28, 2006


Power Up Strappings :
SUSA# :
Integrated LAN Reset method
1 : For desktop
0 : For notebook
(without wake on LAN feature from S4 / S5)
-PCS_3 | VKCOMP for Vlink at 4x mode
0 | 0.75V
1 | 0.9V
GPIOA GPIOC | HOST CLOCK
1 | AUTO MODE
GPIOB | IOQ Depth
0 | 8 Level
1 | 1 Level
GPIOD | GTL pullup
0 | Enable
1 | Disable
PD_A0 | Vlink auto compensation
0 | Auto mode
1 | Manual mode
Digital Power
Analog PWR
Primary IDE Interface
Secondary IDE Interface
Serial ATA Interface
HD Audio / AC97 Audio
Power Management and Event Detection
(SMB) Interface (I2C Bus)
PC / PCI DMA
PLL
Analog GND
Digital GND
AP339E
AP339G
IDE
STX SRX
20 // 5 / 7 / 5 // 20
Solder side
near chipset
VT8237A N/A AP339E
AP339E page 4 SEEDIN
MICRO-START INT'L CO.,LTD.
VT-8251L IDE & SATA & SMB & HDA
MS-7318-0B-060828E
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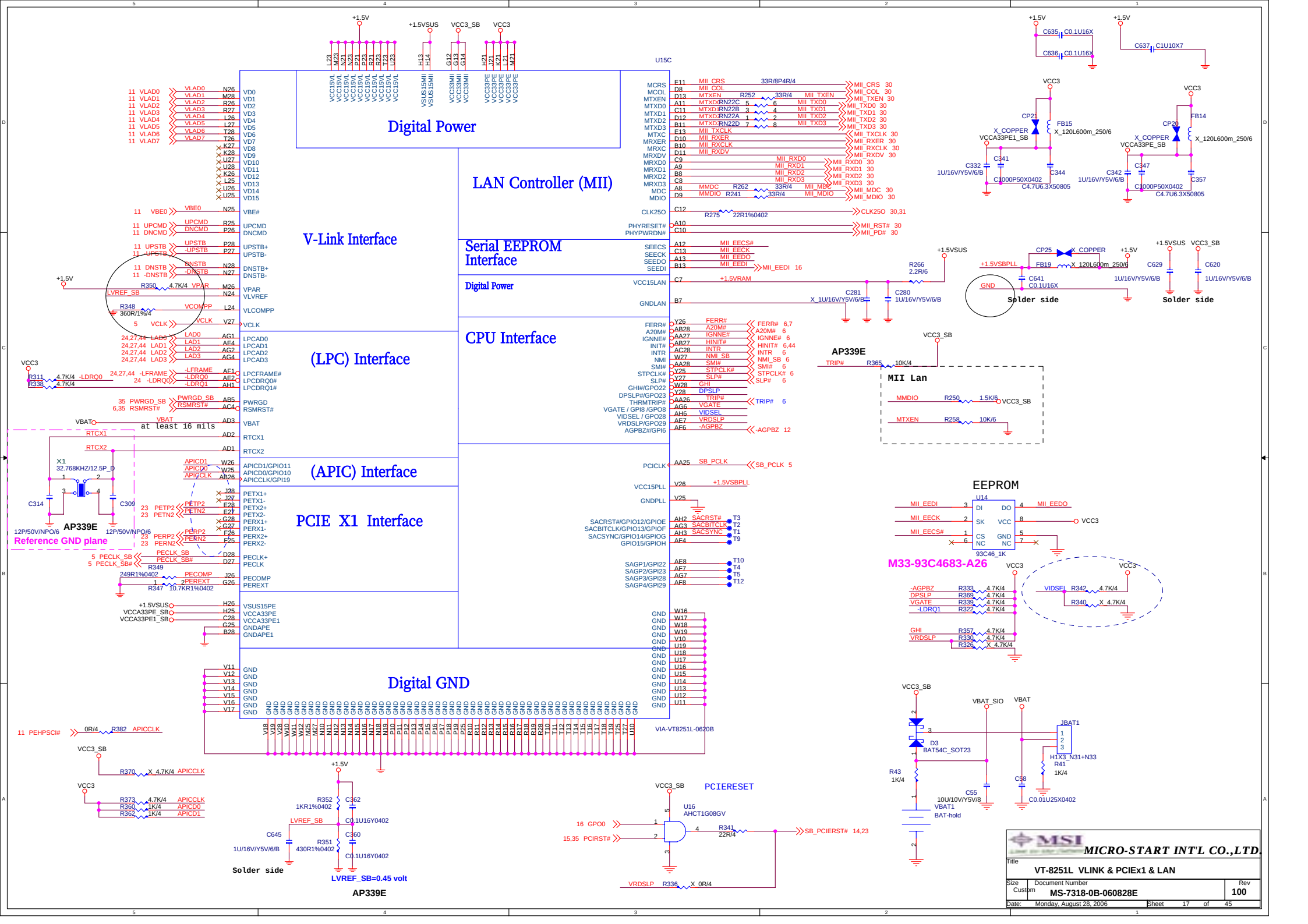
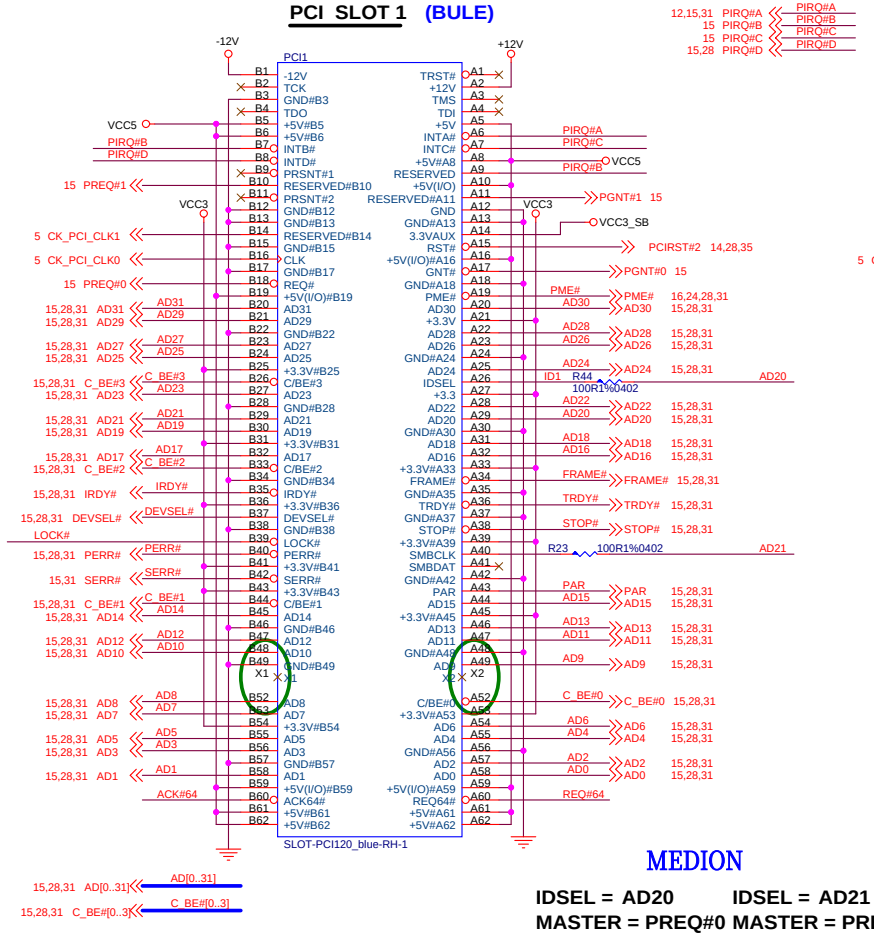
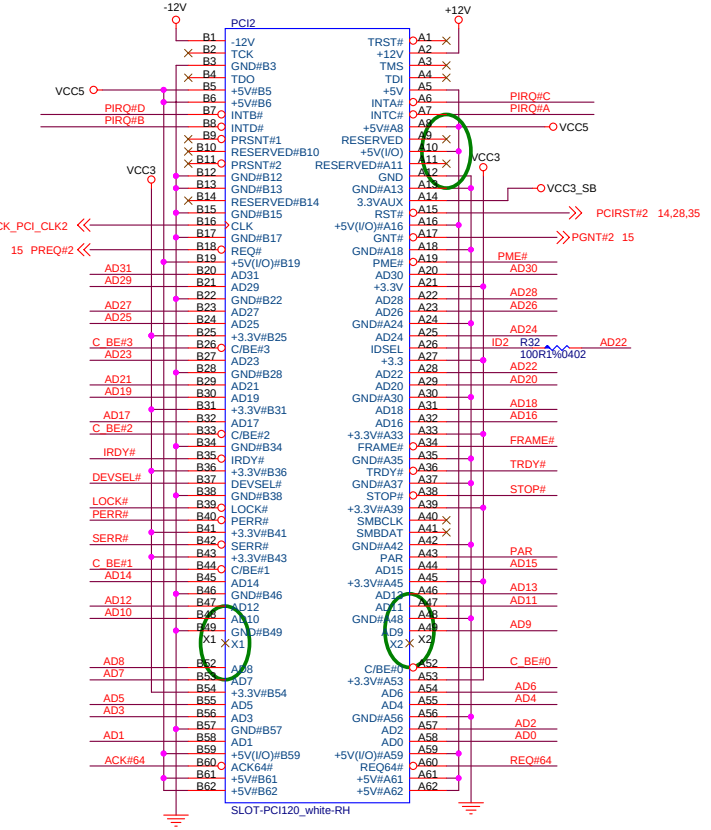

Digital Power
LAN Controller (MII)
V-Link Interface
Serial EEPROM Interface
Digital Power
CPU Interface
(LPC) Interface
(APIC) Interface
PCIE X1 Interface
Digital GND
U15C
AP339E
MII Lan
EEPROM
M33-93C4683-A26
93C46_1K
Solder side
Reference GND plane
LVREF_SB=0.45 volt
PCIERESET
MICRO-START INT'L CO.,LTD.
VT-8251L VLINK & PCIEx1 & LAN
MS-7318-0B-060828E
Monday, August 28, 2006

PCI SLOT 1 (BULE)



PCI SLOT 2



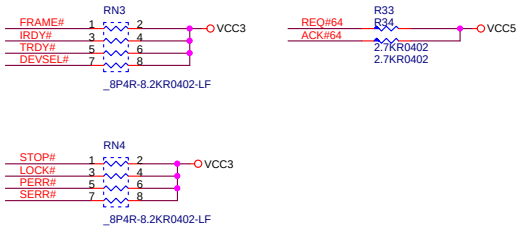
MEDION

IDSEL = AD20
MASTER = PREQ#0
PIRQ#A
CK_PCI_CLK0

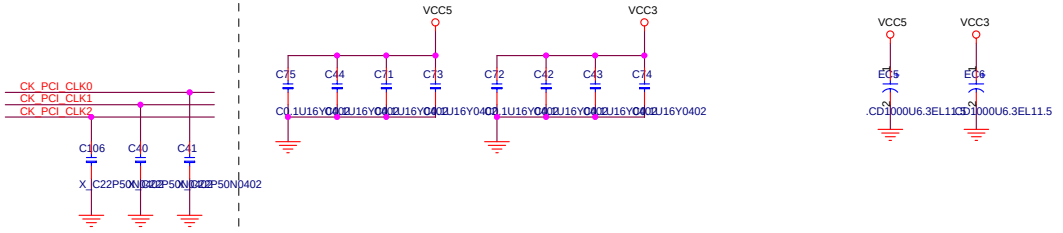
IDSEL = AD21
MASTER = PREQ#1
PIRQ#B
CK_PCI_CLK1

IDSEL = AD22
MASTER = PREQ#2
PIRQ#C
CK_PCI_CLK2

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



Title	PCI Slot
Size	Custom
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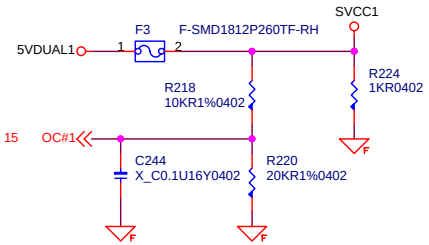
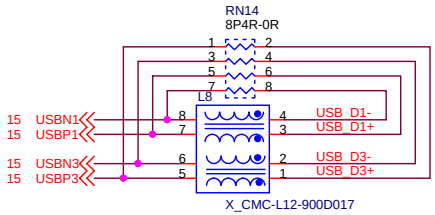
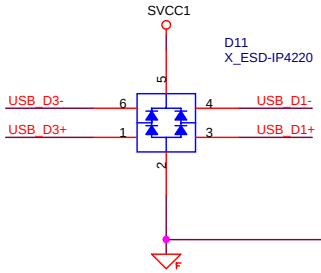
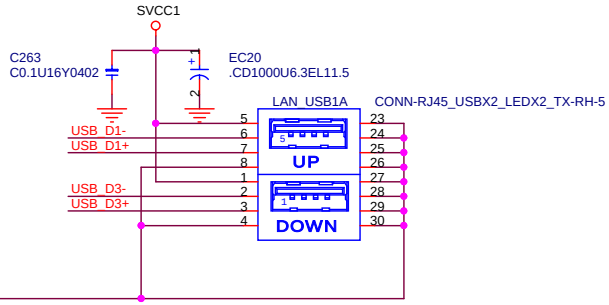
MICRO-START INT'L CO.,LTD.

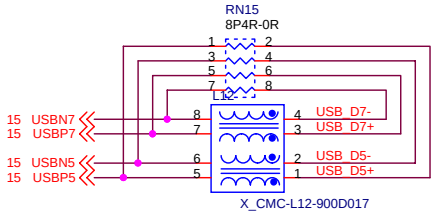
USB Rear Connector

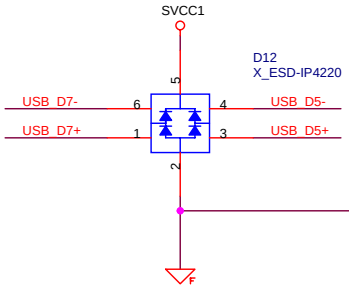


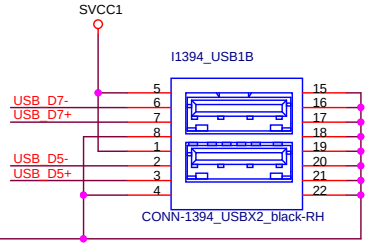












MICRO-START INT'L CO.,LTD.

Title	USB Connectors -> Real	
Size	Document Number: MS-7318-0B-060828E	Rev: 100
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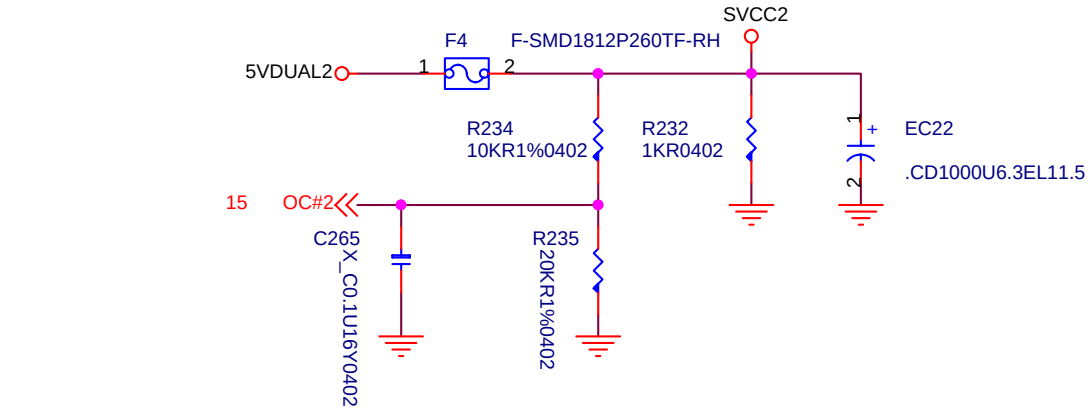

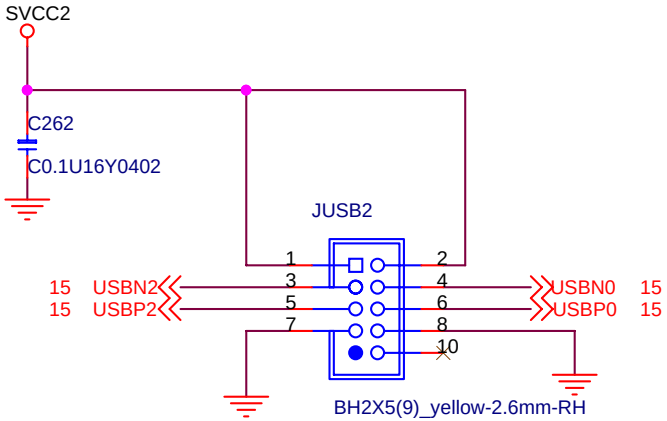

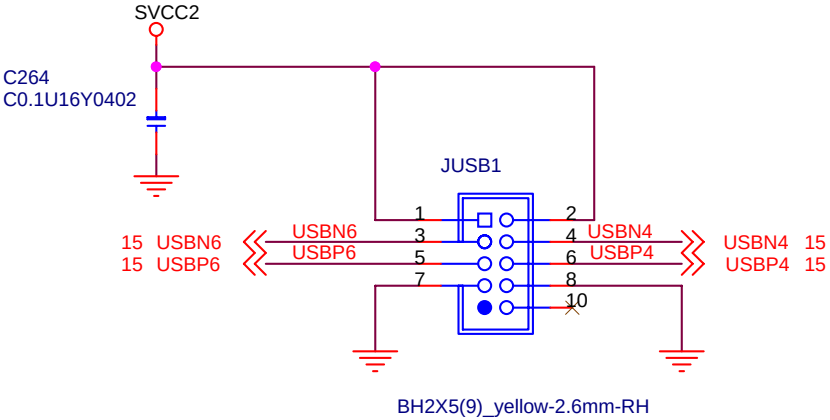

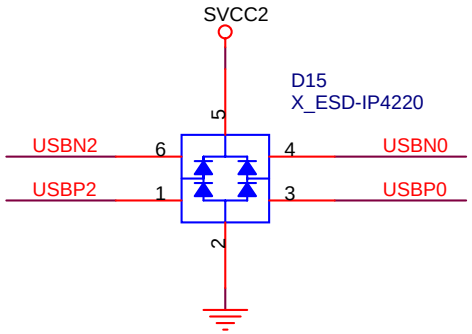

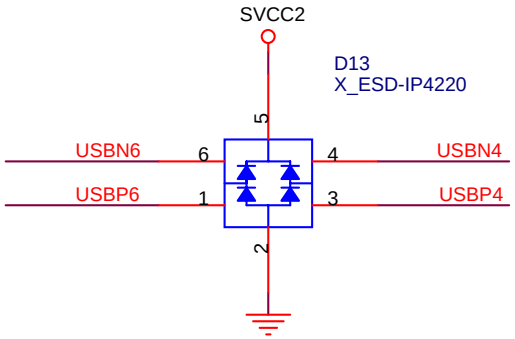

JUSB1, JUSB2

PIN1	VCC#1	PIN2	VCC#2
PIN3	USB0-	PIN4	USB1-
PIN5	USB0+	PIN6	USB1+
PIN7	GND7	PIN8	GND8
PIN9	KEY	PIN10	USBOC

MICRO-START INT'L CO.,LTD.

Title: **USB Connectors -- Front**

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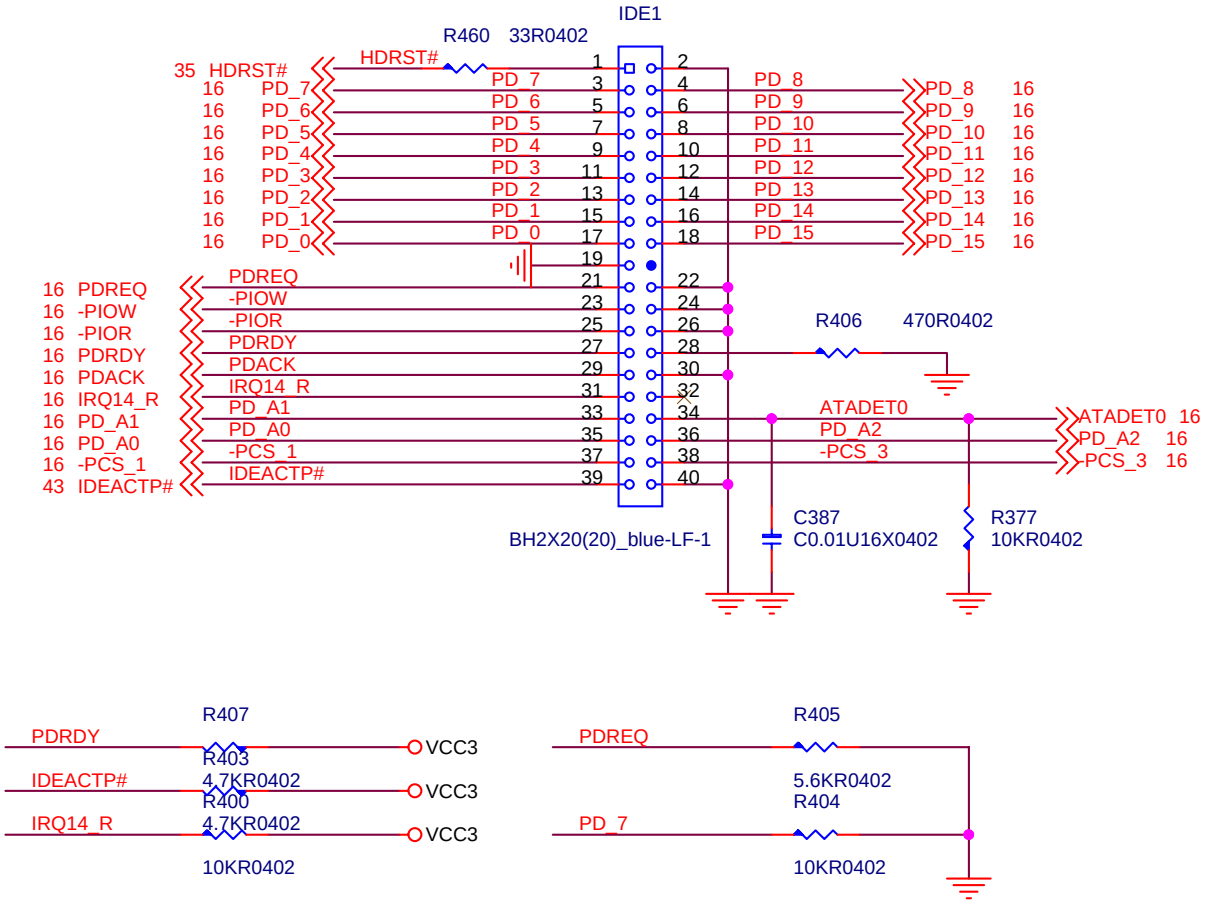
IDE Connector



MICRO-START INT'L CO.,LTD.

Title	SATA & IDE CONNECTOR	
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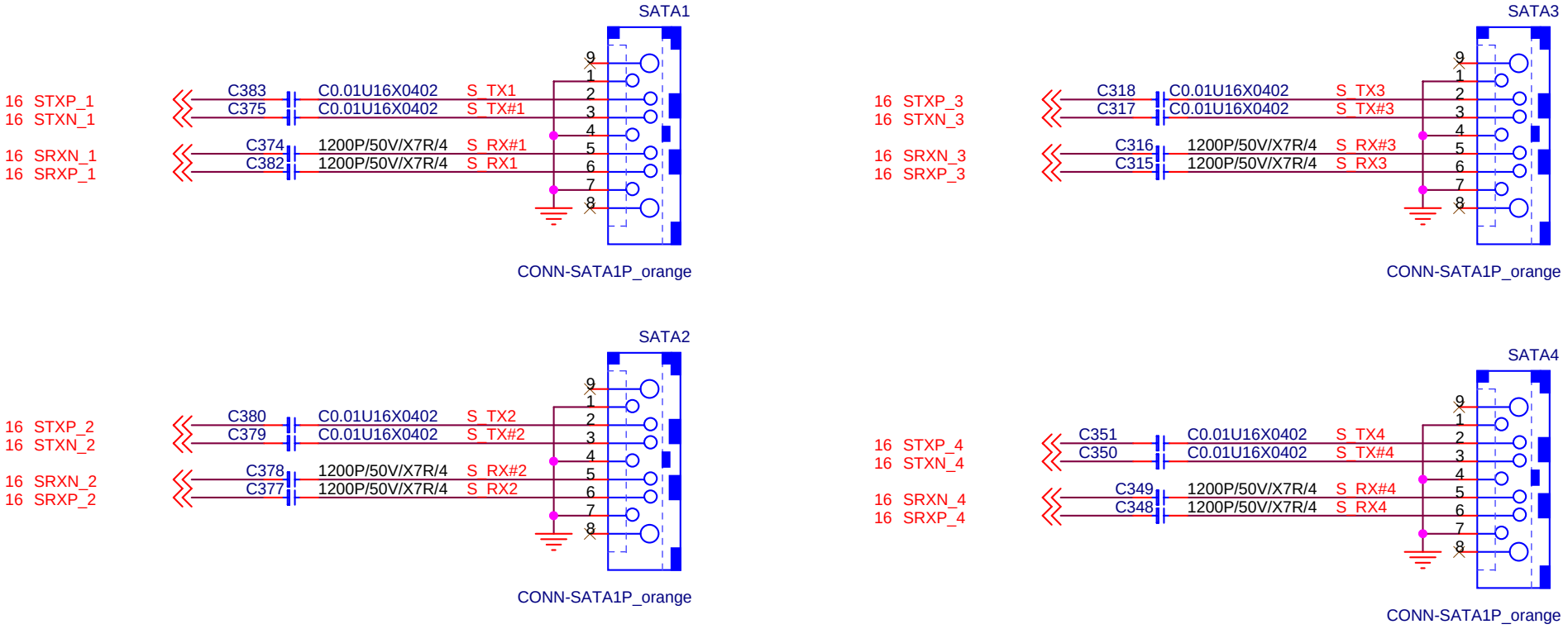
SATA Connector



MICRO-START INT'L CO.,LTD.

Title: SATA & IDE CONNECTOR

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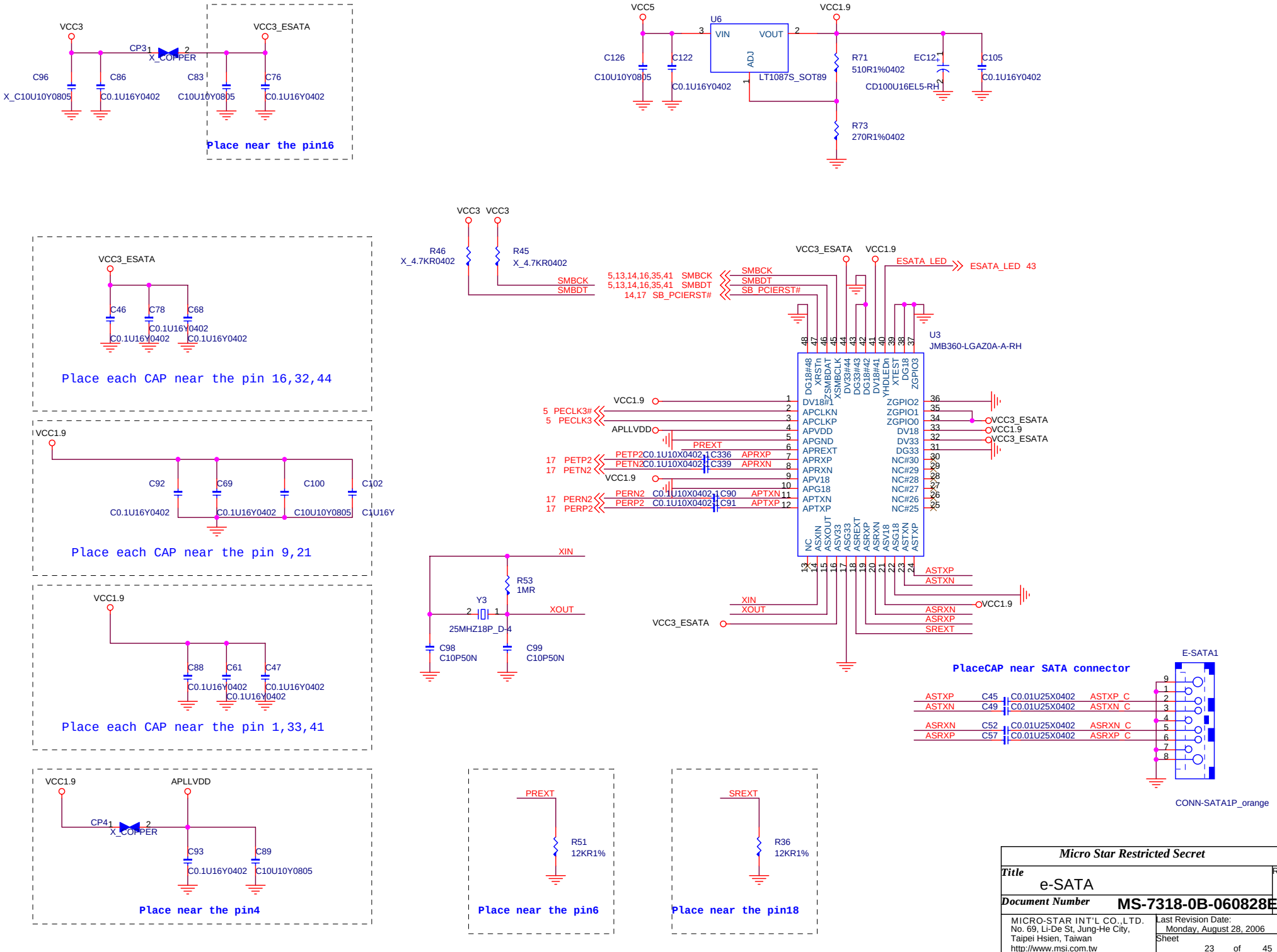

Micro Star Restricted Secret

Title e-SATA	Rev 100
Document Number MS-7318-0B-060828E	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Monday, August 28, 2006
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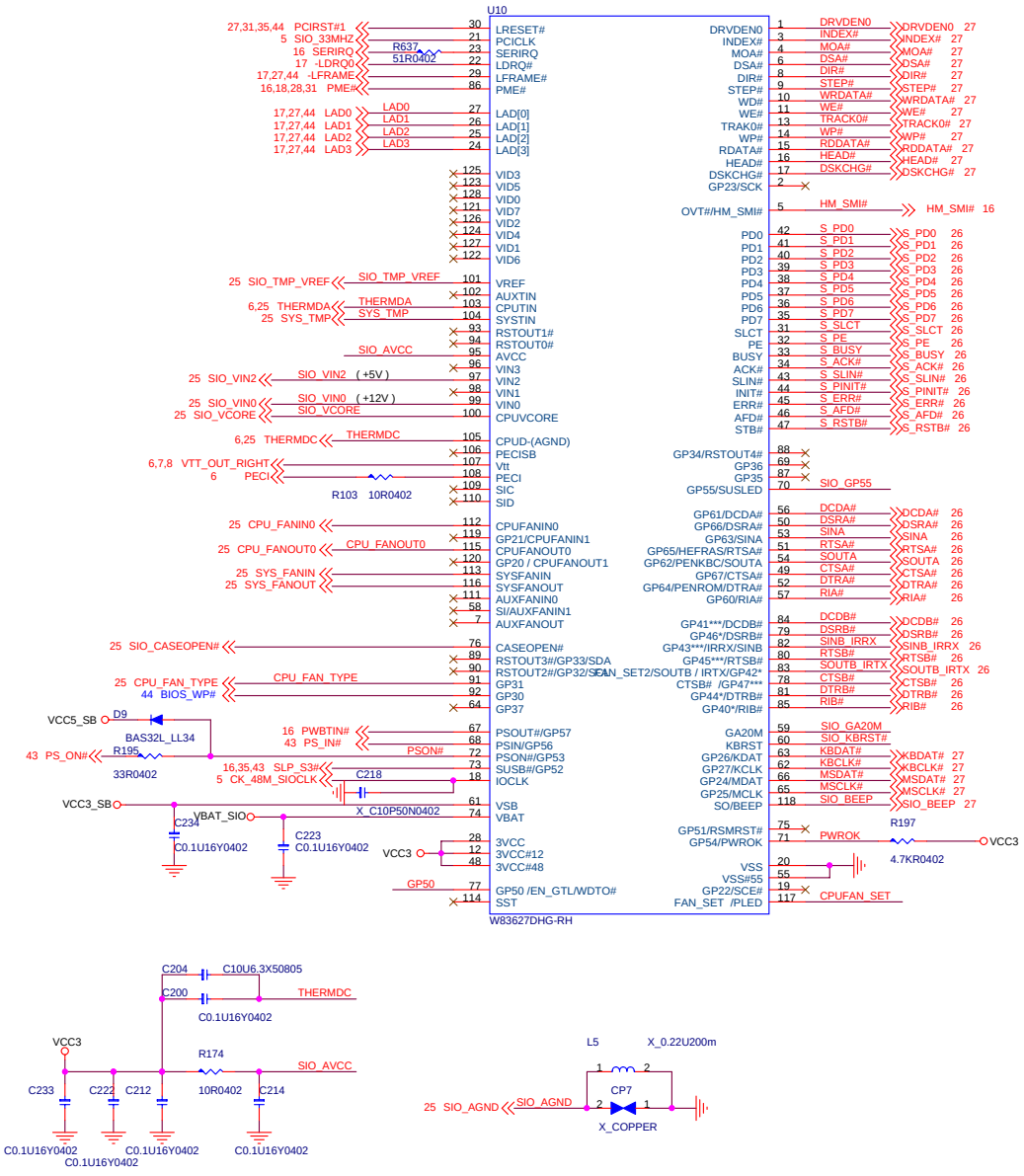
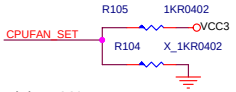
LPC SUPER I/O W83627DHG



FAN_SET : (117, Internal pull down)



High : 100%

Low: 50%

Note : For CPUFANOUT0 only

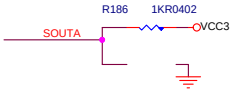
FAN_SET2 : (83, Internal pull down)

High : 100%

Low: 50%

Note : For CPUFANOUT1 only

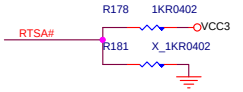
Keyboard Enable/Disable : (54)



High : Enable

Low: Disable

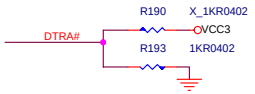
Configration Address Select : (51)



High : 4E

Low: 2E

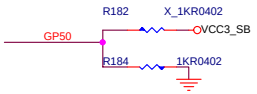
ROM Enable/Disable : (52)



High : Enable

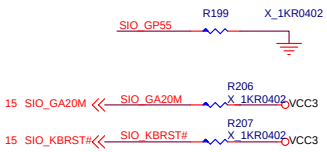
Low: Disable

VID Level Select : (77)



High : Enable

Low: Disable



MICRO-START INT'L CO.,LTD.

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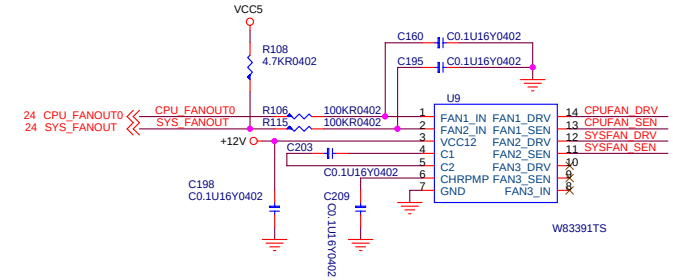
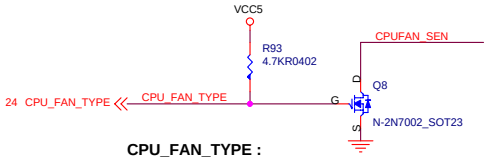
DC FAN Controllor

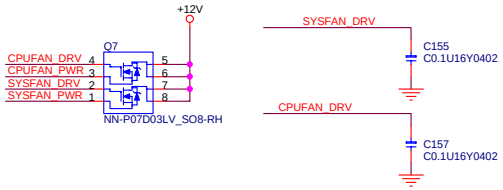




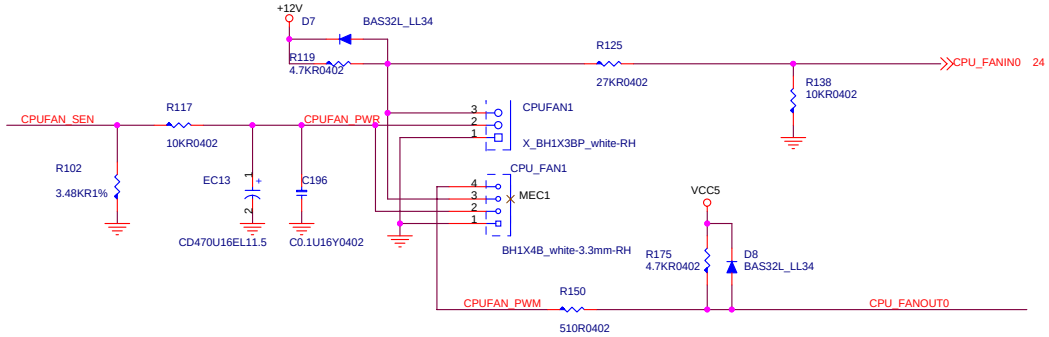
CPU_FAN_TYPE :

High : 4-pin

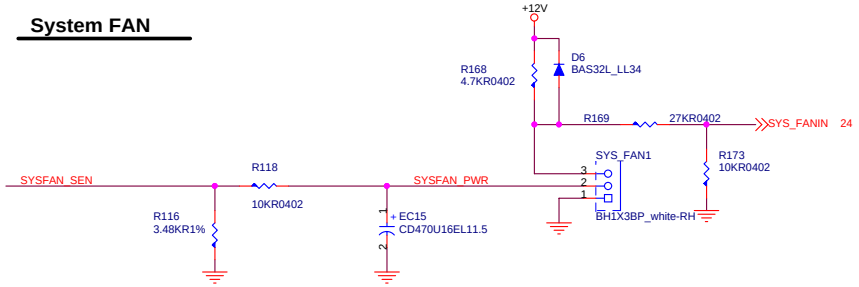
Low : 3-pin



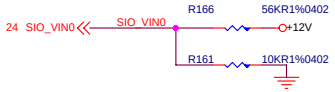
CPU FAN

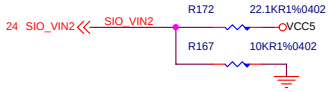


System FAN

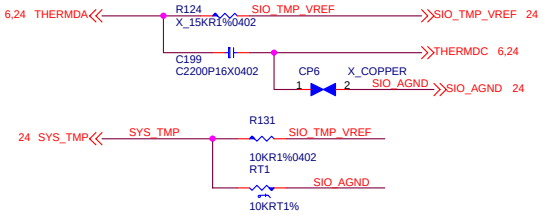


Voltage Monitor

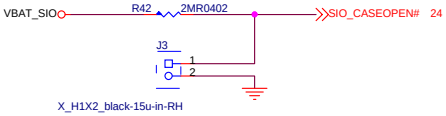




Thermal Monitor



Case Open



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Title	SIO_Hardware Monitor	
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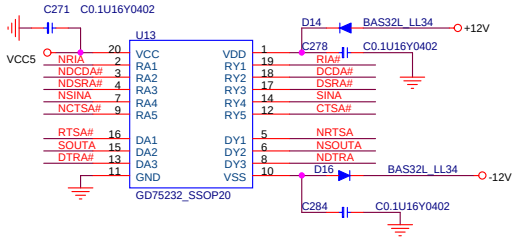
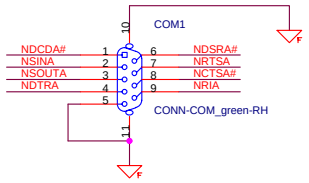
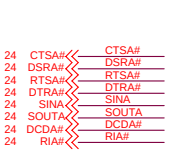
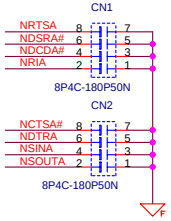
SERIAL PORT 1

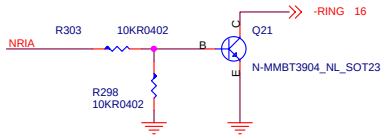




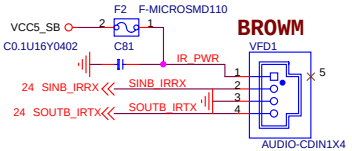


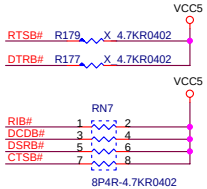


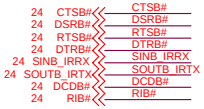
WAKE ON RING



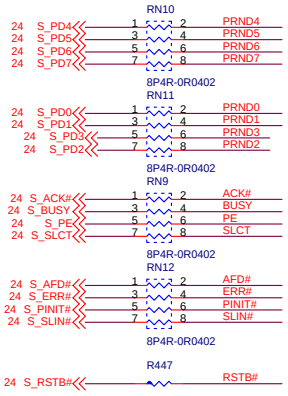
Front LCD (SERIAL PORT 2)

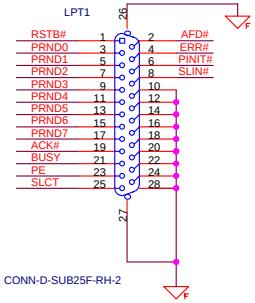


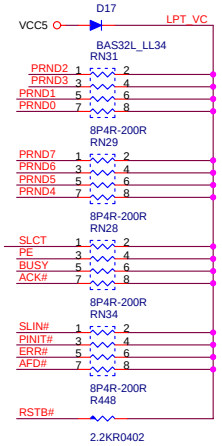


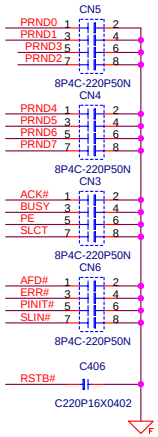


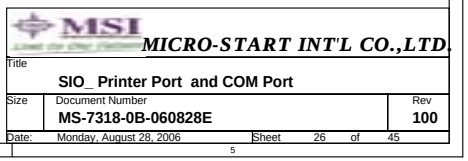
PARALLAL PORT



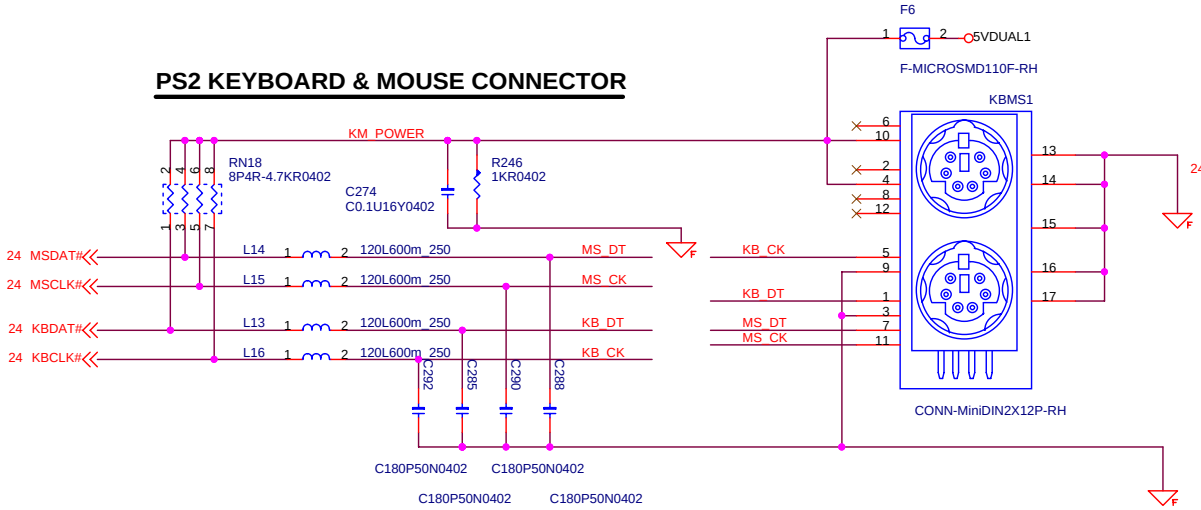




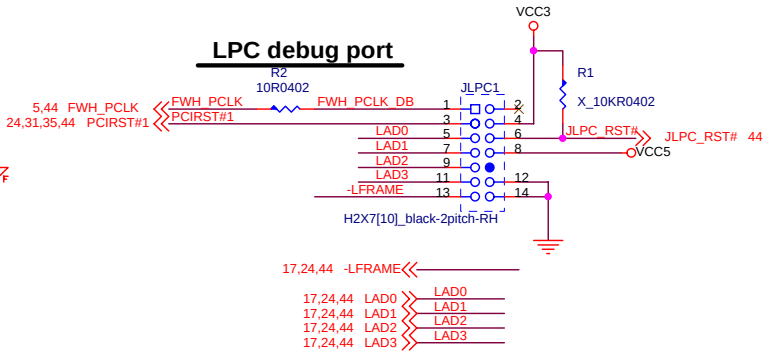




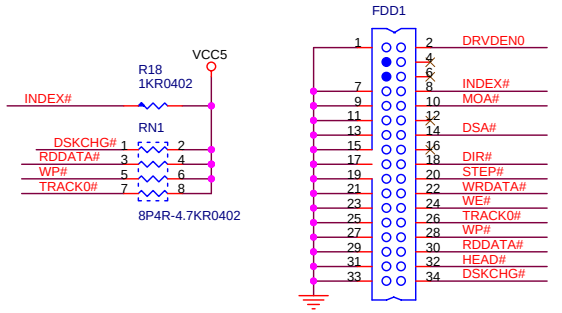
PS2 KEYBOARD & MOUSE CONNECTOR

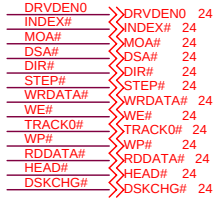


LPC debug port

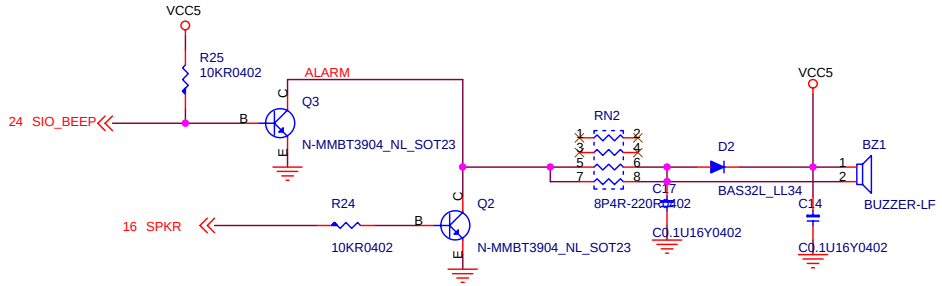


FLOPPY CONNECTOR





BUZZER



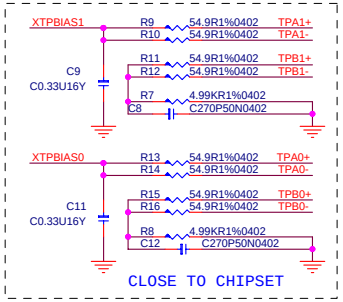
MICRO-START INT'L CO.,LTD.

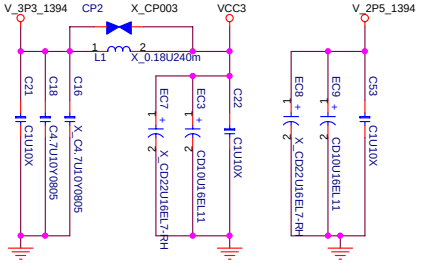
Title	SIO_KB, FDD, LPC Debug Port	
Size B	Document Number MS-7318-0B-060828E	Rev 100
Date: Monday, August 28, 2006	Sheet 27 of 45	

1394 VT6308P

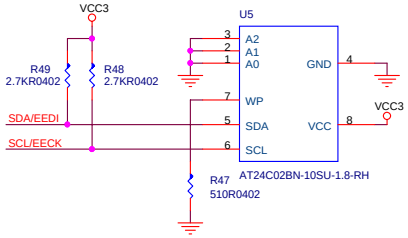
	VCC3	V_3P3_1394	V_2P5_1394	BUS_PWR
VT6308P	3.3V	3.3V	2.5V	12V

VCC POWER SOUCE

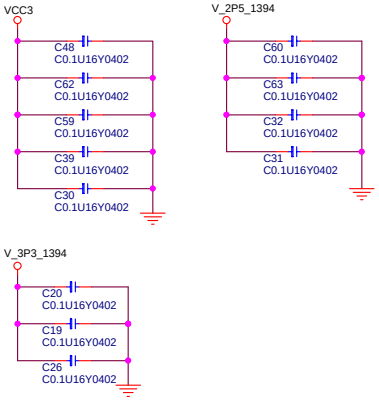


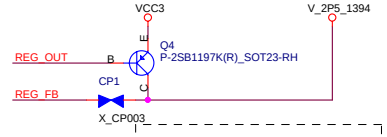


1394-EEPROM 24C02



Decouping Cap.





BJT_CTL
0 : Internal power MOS
1 : External BJT

When cable power exists
XCPS status is 1

I2C EEPROM ENABLE Pull High

Pull high to PHY digital power
EEPROM auto loading will disable

PIN 62,65,75,76,89,90 Analog Power(3.3V)
PIN 33 Internal SRAM Power(2.5V)
PIN 24,49,114 Core Power(2.5V)
PIN 8,20,39,102,113,125 I/O Power(3.3V)

15,18,31 AD[0..31] AD[0..31]
15,18,31 C_BE#[0..3] C_BE#[0..3]

IDSEL = AD23
MASTER = PREQ#3
PIRQ#D

MICRO-START INT'L CO.,LTD.

Title: 1394-VT6308P		
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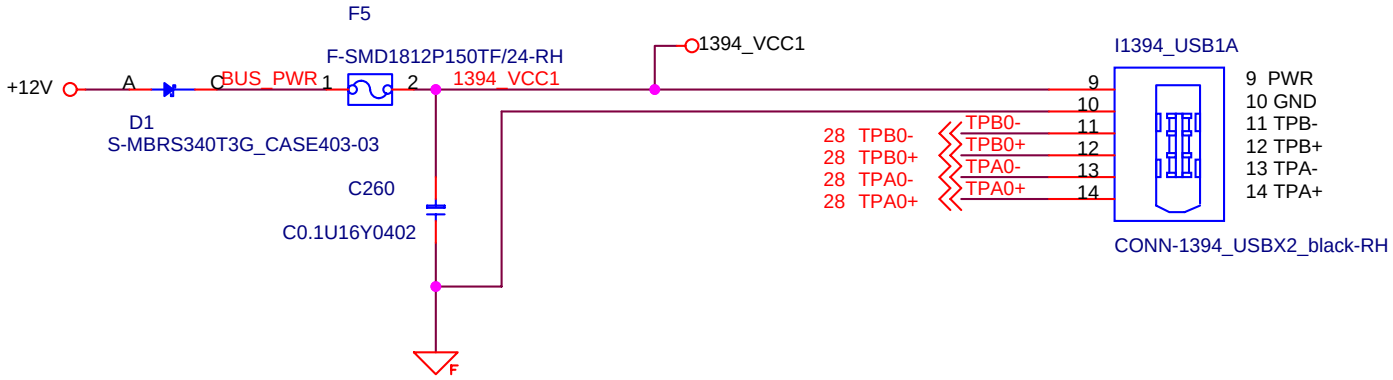
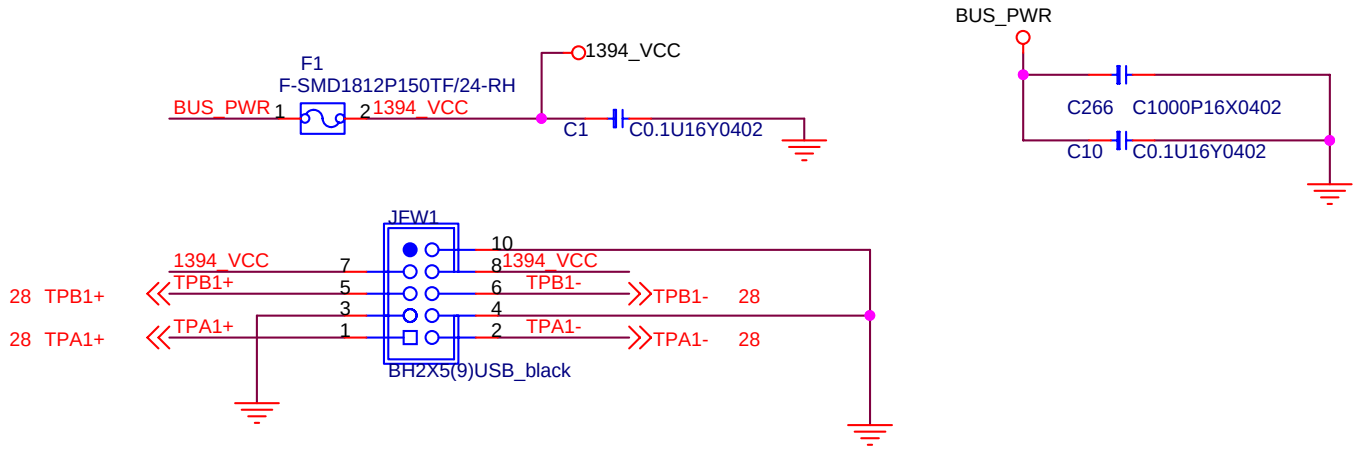
REAR 1394 PORT



FRONT 1394 PORT



Title: 1394 PORT		
Size: A	Document Number: MS-7318-0B-060828E	Rev: 100
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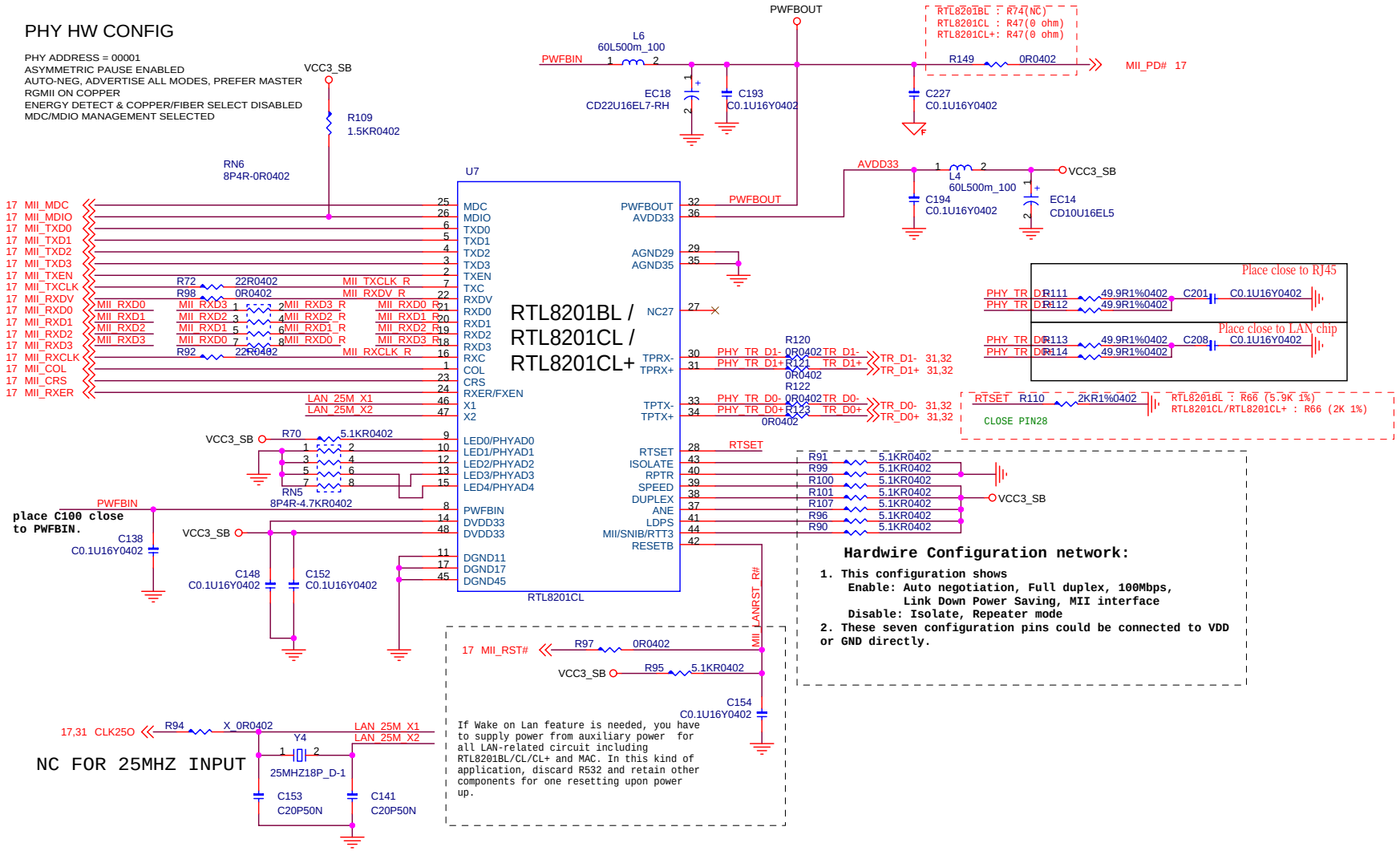
PWFBOUT is 1.8V voltage outpt.
EC6 TCAP 22uF change ECAP 100uF
Place L11 close to PWFBOUT

PHY HW CONFIG

PHY ADDRESS = 00001
ASYMMETRIC PAUSE ENABLED
AUTO-NEG, ADVERTISE ALL MODES, PREFER MASTER
RGMII ON COPPER
ENERGY DETECT & COPPER/FIBER SELECT DISABLED
MDC/MDIO MANAGEMENT SELECTED



MII_MDC	MII_MDIO	MII_TXD0	MII_TXD1
MII_TXD2	MII_TXD3	MII_TXEN	MII_TXCLK
MII_RXDV	MII_RXD0	MII_RXD1	MII_RXD2
MII_RXD3	MII_RXCLK	MII_COL	MII_CRS
MII_RXER			

R72 22R0402 MII_TXCLK_R
R98 0R0402 MII_RXDV_R
MII_RXD3 MII_RXD3_R
MII_RXD2 MII_RXD2_R
MII_RXD1 MII_RXD1_R
MII_RXD0 MII_RXD0_R
R92 22R0402 MII_RXCLK_R

LAN_25M_X1
LAN_25M_X2

MDC	MDIO	TXD0	TXD1
TXD2	TXD3	TXEN	TXC
RXDV	RXD0	RXD1	RXD2
RXD3	RXC	COL	CRS
RXER/FXEN	X1	X2	
LED0/PHYAD0	LED1/PHYAD1	LED2/PHYAD2	LED3/PHYAD3
LED4/PHYAD4	PWFBIN	DVDD33	DVDD33
DGND11	DGND17	DGND45	

PWFBOUT	AVDD33	AGND29	AGND35
NC27	TPRX-	TPRX+	TPTX-
TPTX+	RTSET	ISOLATE	RPTR
SPEED	DUPLEX	ANE	LDPS
MII/SNIB/RTT3	RESETB		

PHY_TR_D1- TR_D1- TR_D1- 31,32
PHY_TR_D1+ TR_D1+ TR_D1+ 31,32
PHY_TR_D0- TR_D0- TR_D0- 31,32
PHY_TR_D0+ TR_D0+ TR_D0+ 31,32

PHY_TR_D1-	PHY_TR_D1+	PHY_TR_D0-	PHY_TR_D0+

TR_D1- 31,32	TR_D1+ 31,32	TR_D0- 31,32	TR_D0+ 31,32

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Size B	Document Number MS-7318-0B-060828E		Rev 100
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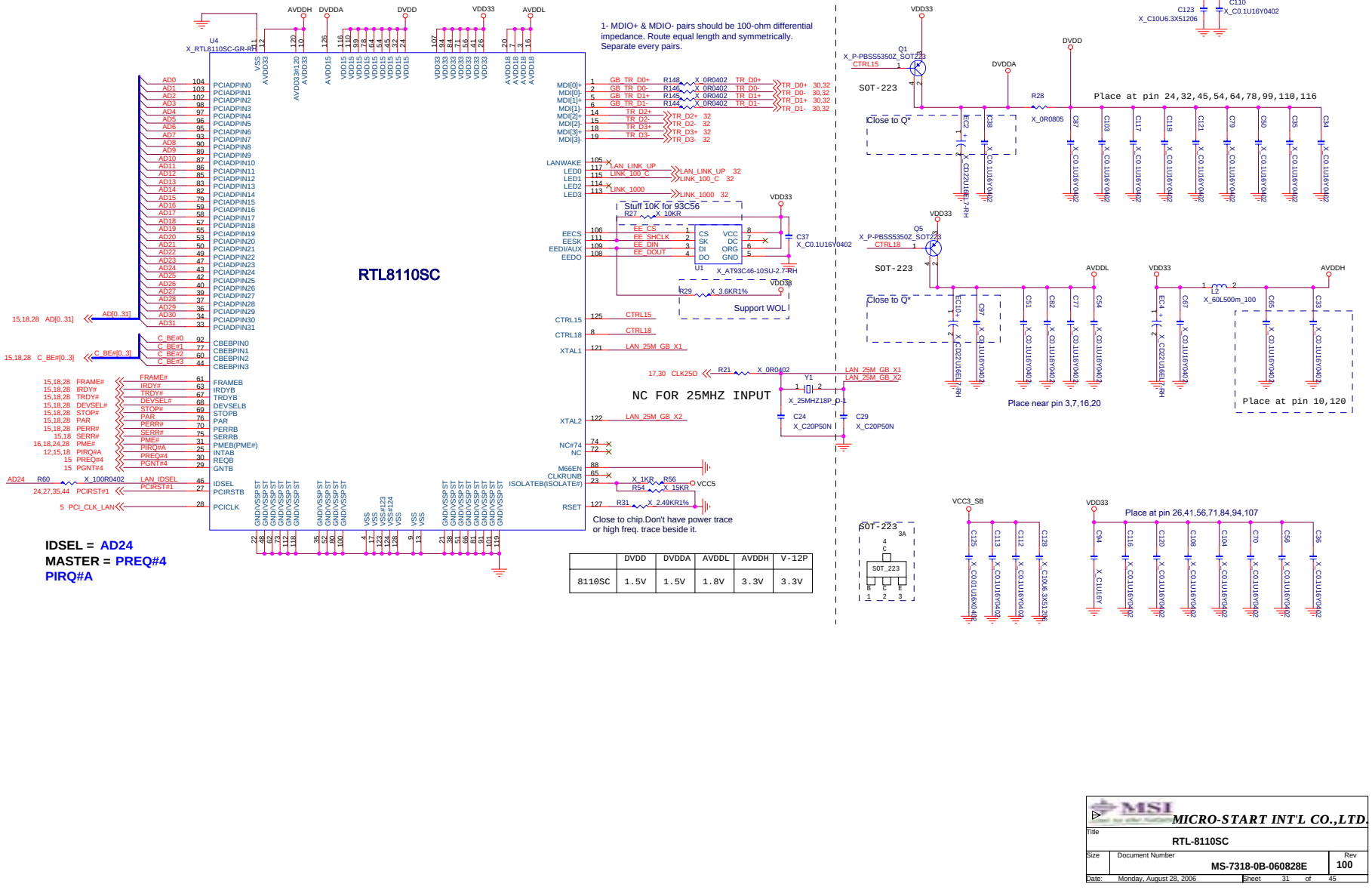

	DVDD	DVDDA	AVDDL	AVDDH	V-12P
8110SC	1.5V	1.5V	1.8V	3.3V	3.3V

MICRO-START INT'L CO.,LTD.

Title	RTL-8110SC	
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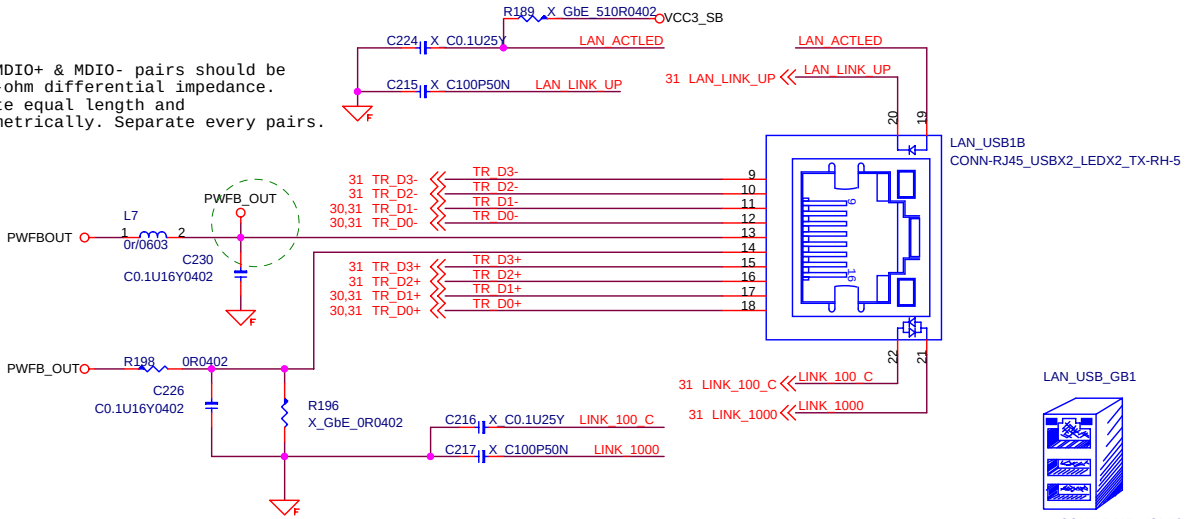
RJ45 Connector (with transformer)

LAN Interface
Diff. Trace width 8 mils & 8 mils space.
Diff. & other space 40 mils.
Length matching: < 10 mils
Ttrace length 0" to 2"

1- MDIO+ & MDIO- pairs should be 100-ohm differential impedance. Route equal length and symmetrically. Separate every pairs.



1G N58-22F0211-S42 : LED RoHS
10/100 N58-18F0081-S42 : Non LED and RoHS

MICRO-START INT'L CO.,LTD.

Title: MS-7318		
Size: B	Document Number: MS-7318-0B-060828E	Rev: 100
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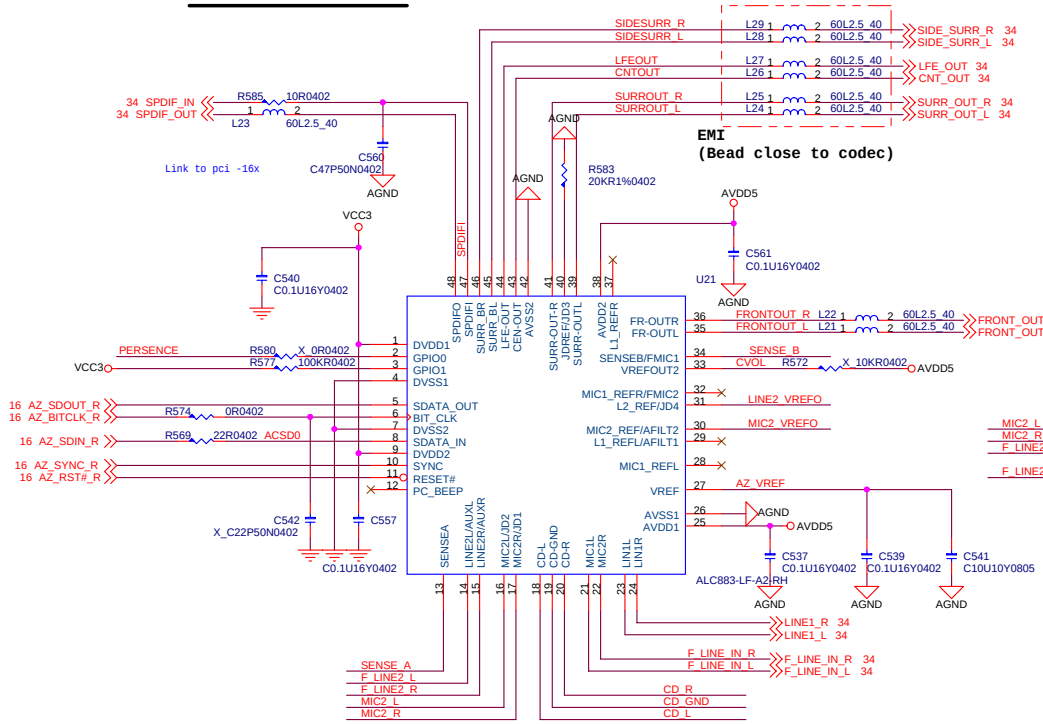
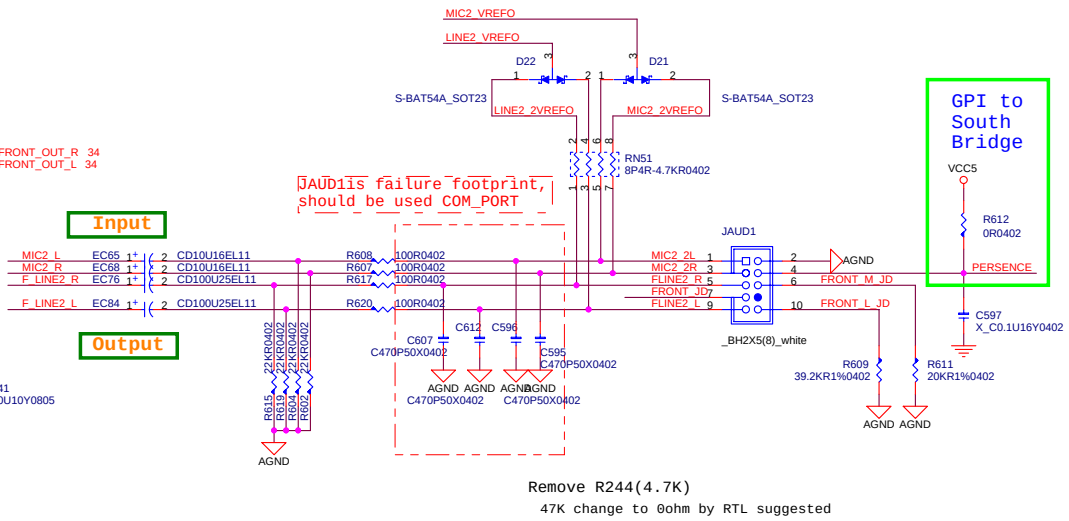
ALC888 CODEC

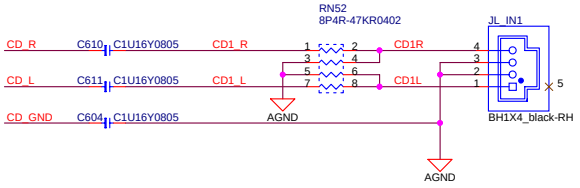


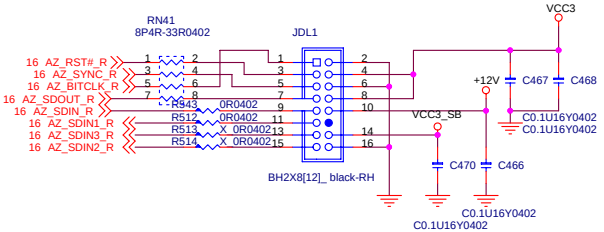
FRONT AUDIO



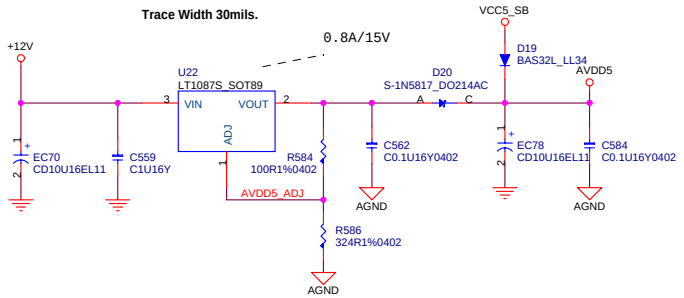
Remove R244(4.7K)
47K change to 0ohm by RTL suggested

RCA Line-in (Input)

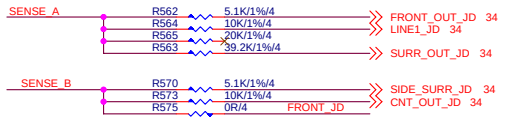




AUDIO CODE REGULATORS



ALC883/888 JACK DETECT



Closer to Codec.

MICRO-START INT'L CO.,LTD.

Title	ALC 888	
Size: Custom	Document Number: MS-7318-0B-060828E	Rev: 100
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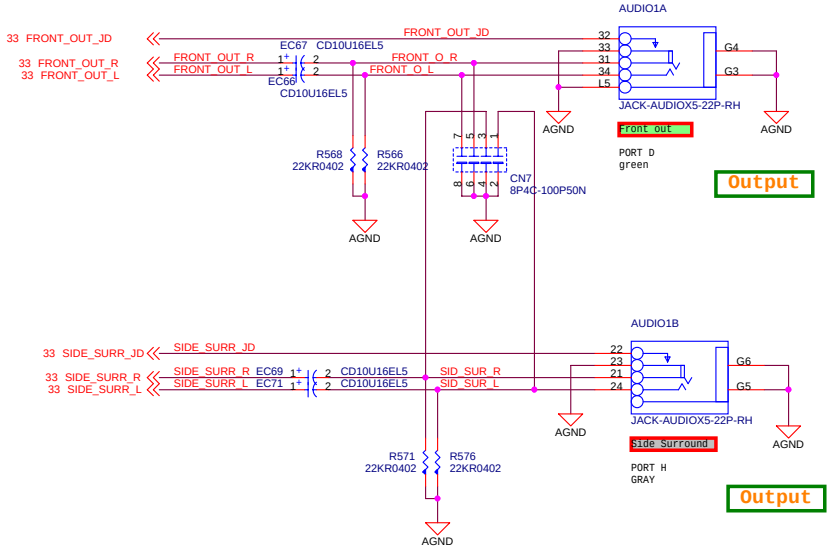
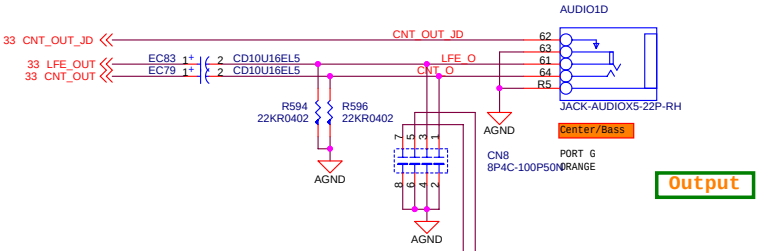
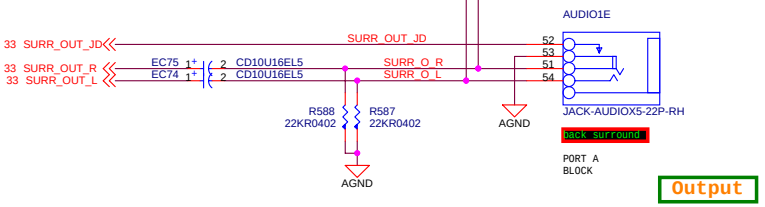
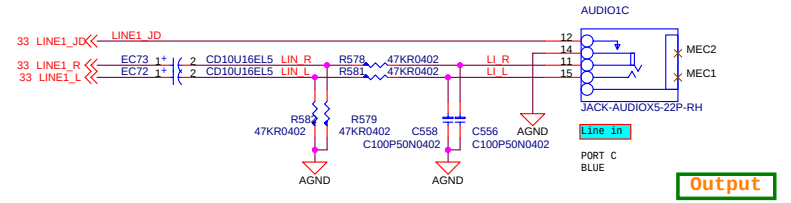
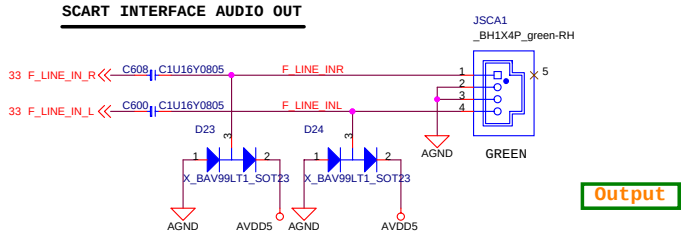
Audio Connector

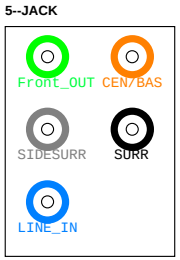


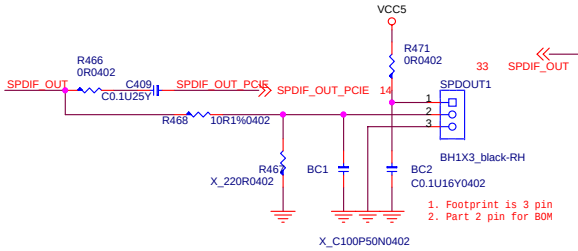


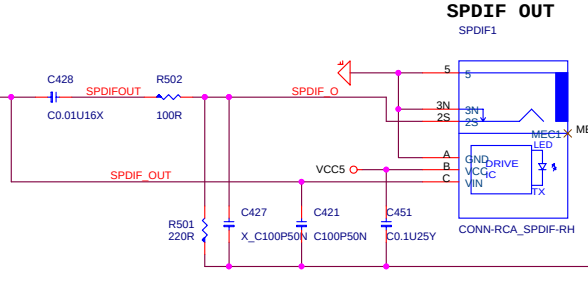


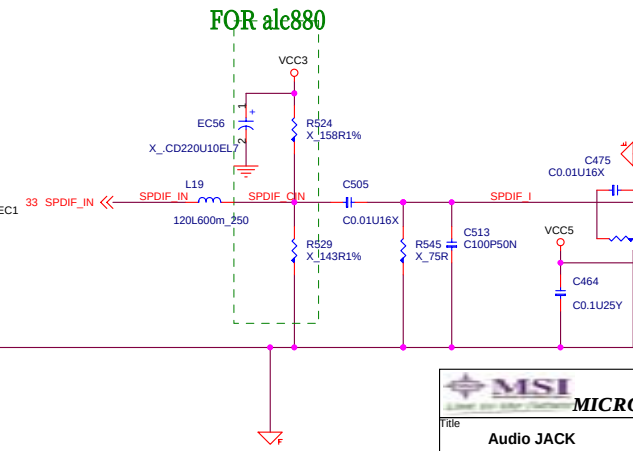


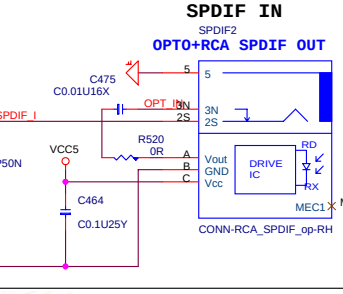












680pF change to 100pF by RTL suggested

MSI MICRO-START INT'L CO.,LTD.

Title: Audio JACK		
Size: Custom	Document Number: MS-7318-0B-060828E	Rev: 100
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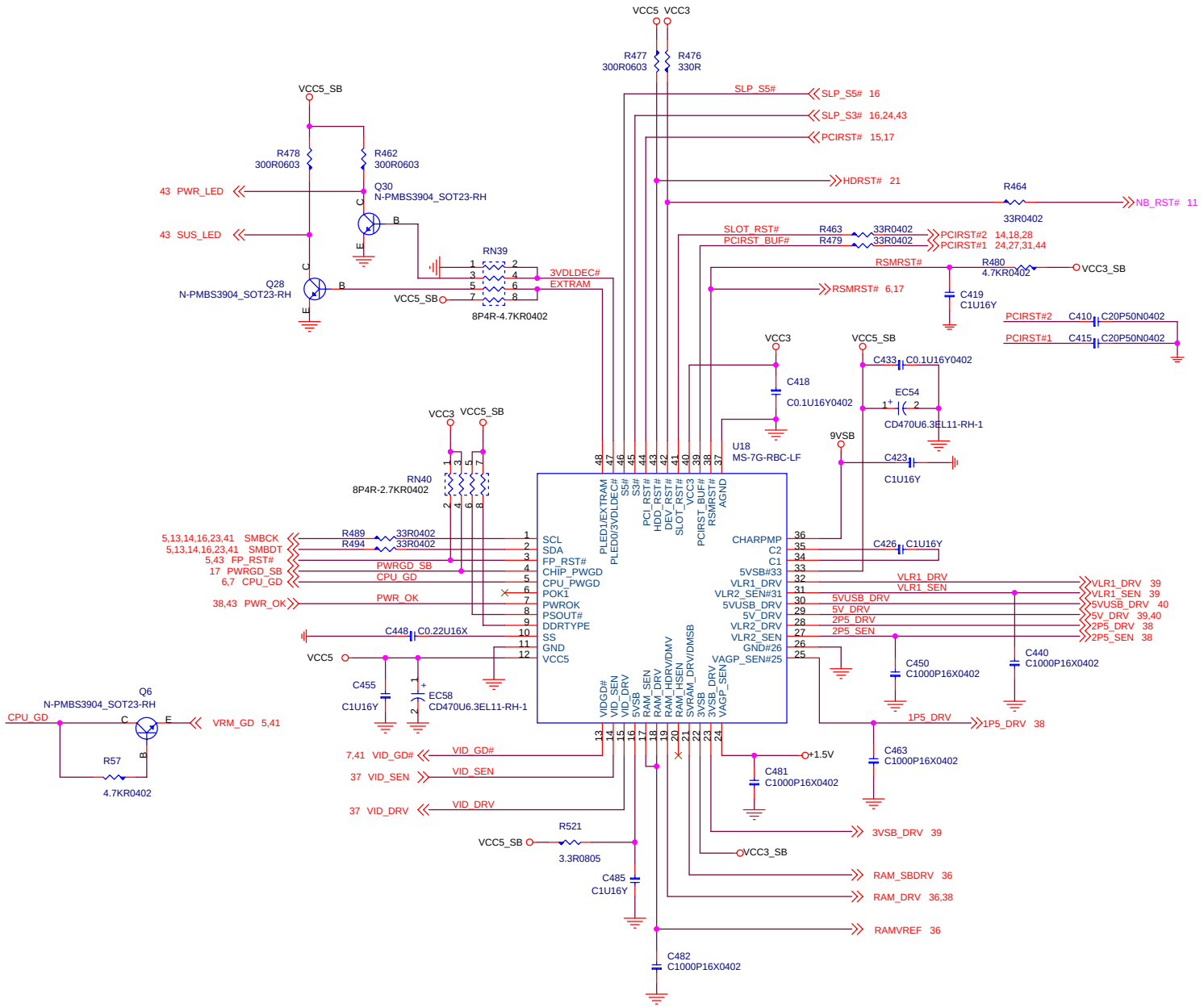

SWITCH:

D03-066880B-F01
D03-06N030B-I14
D03-75N022B-N03
Regulator(TO-252)
D03-45N020B-N03
D03-40N030B-A36
D03-6530A0B-F01
Regulator(TO-263)
D03-50N034B-N03
D03-50N031B-P03
Dual NMOS
D03-07D0303-N03
D03-0731303-A30

MICRO-START INT'L CO.,LTD.

Title: MS-7318		
Size: A3	Document Number: MS-7318-0B-060828E	Rev: 100
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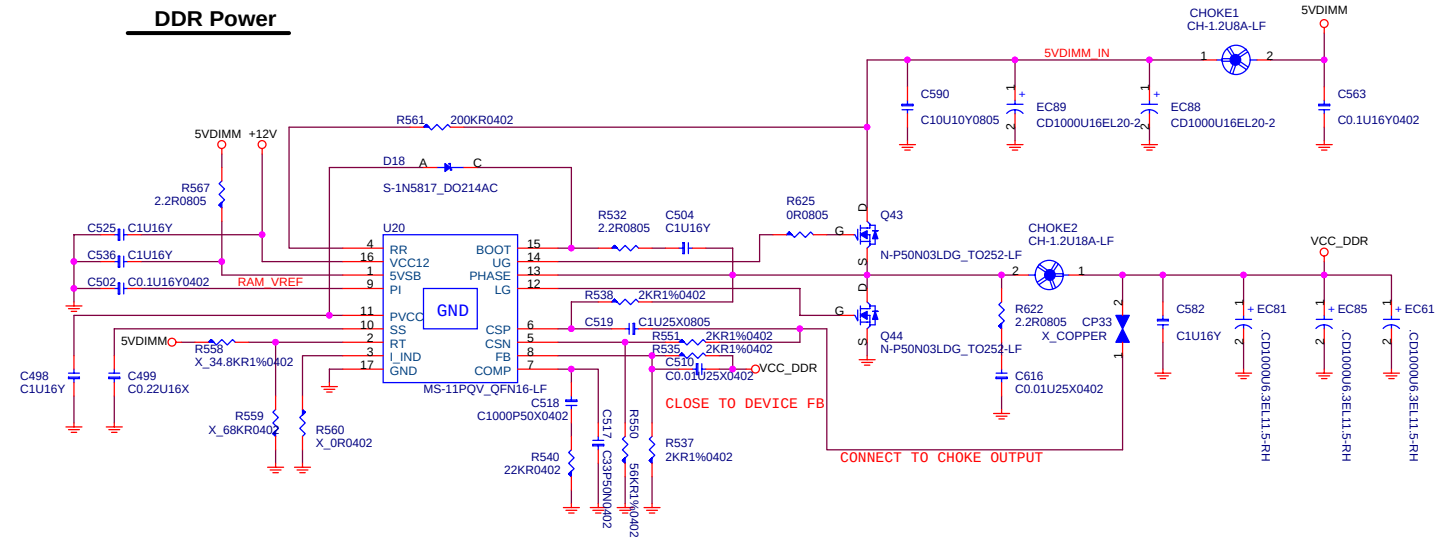
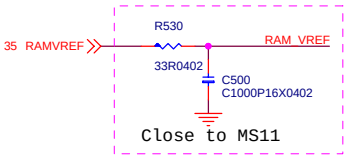
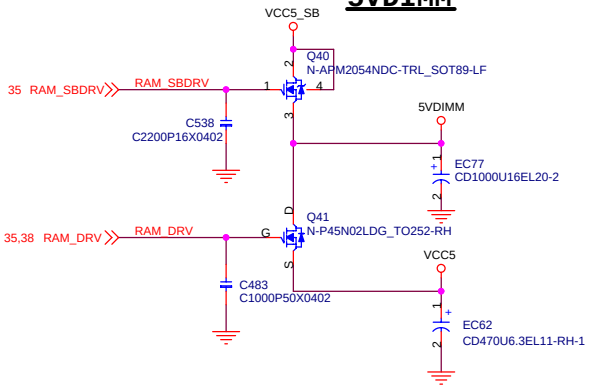
DDR Power

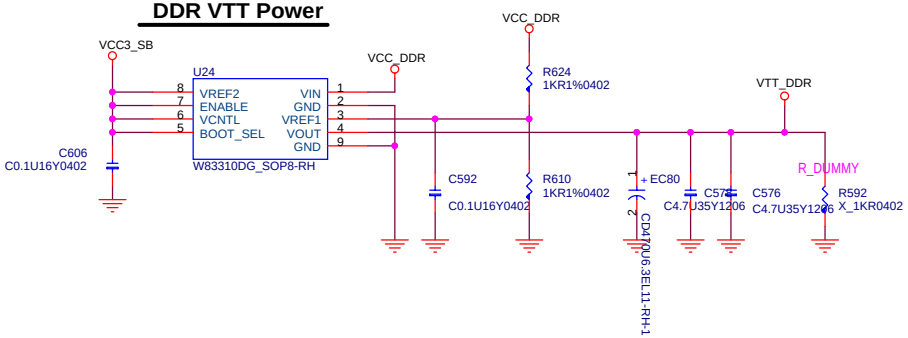




5VDIMM



DDR VTT Power



MICRO-START INT'L CO.,LTD.

Title: MS-7318		
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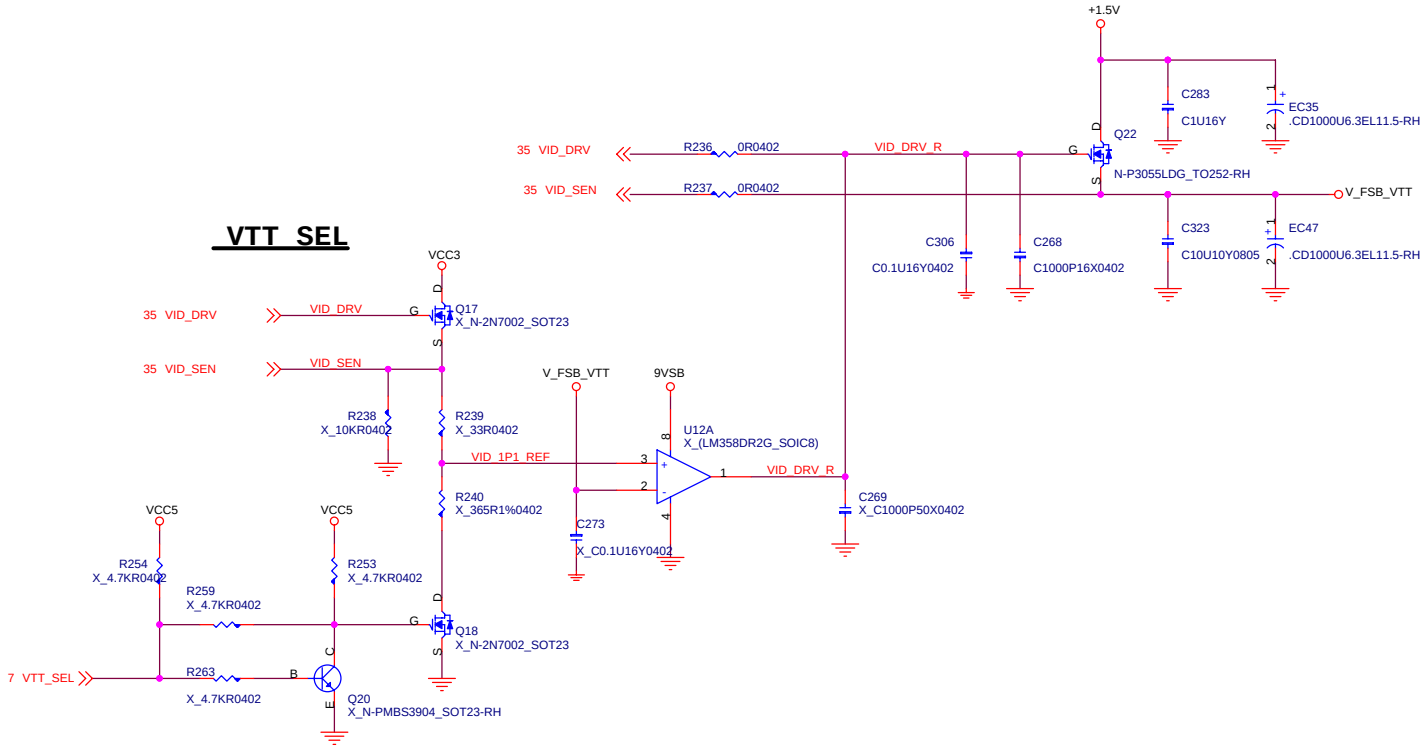

VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.

MICRO-START INT'L CO.,LTD.

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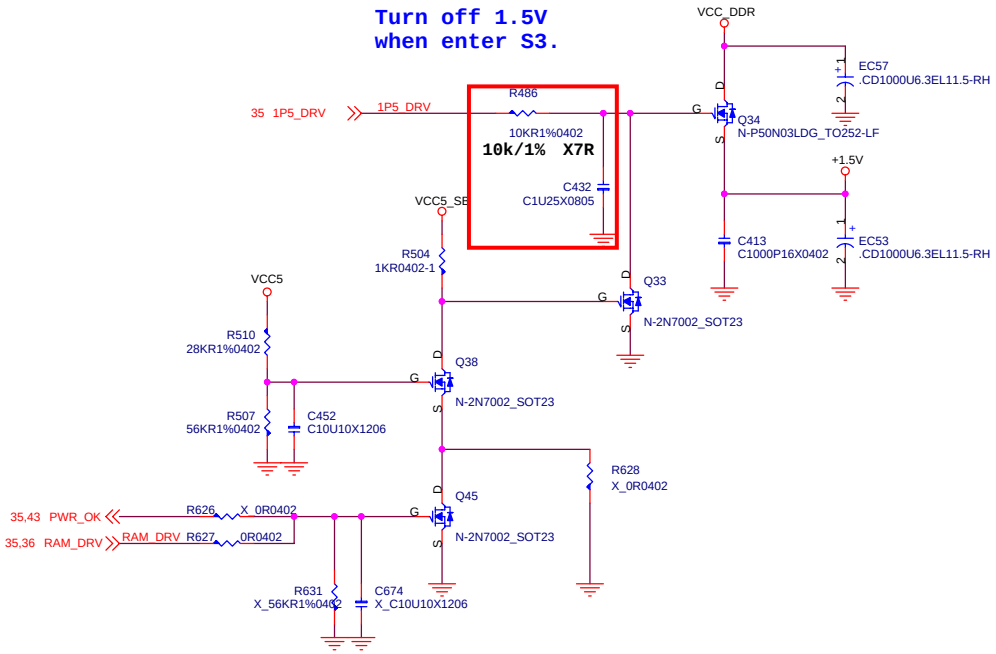
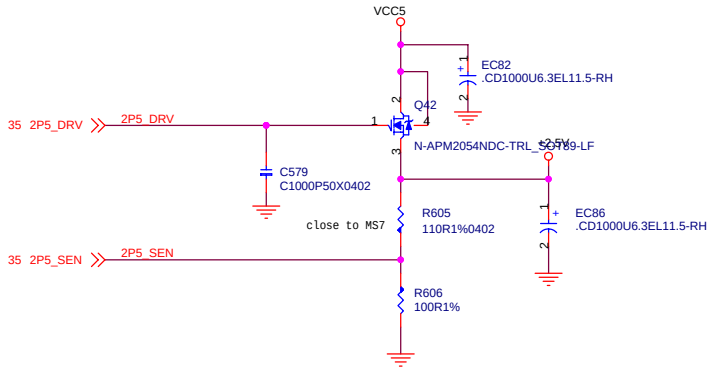
1.5V



2.5V



MICRO-START INT'L CO.,LTD.

Title	MS-7318	
Size A3	Document Number MS-7318-0B-060828E	Rev 100
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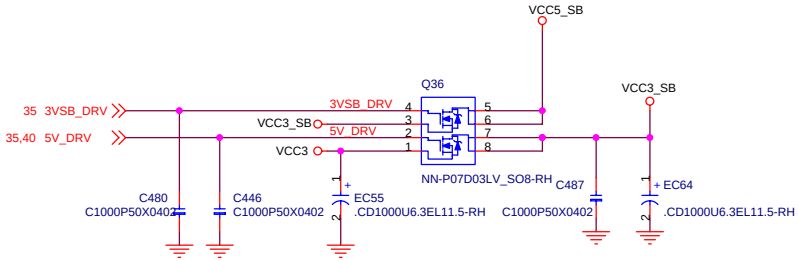
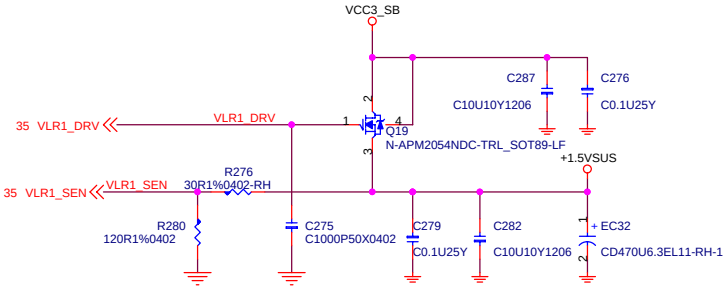


VCC1.5SBY



MICRO-START INT'L CO.,LTD.

Title	MS-7318	
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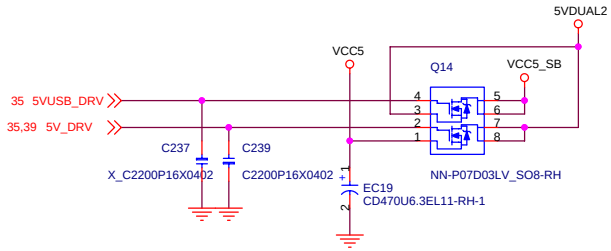
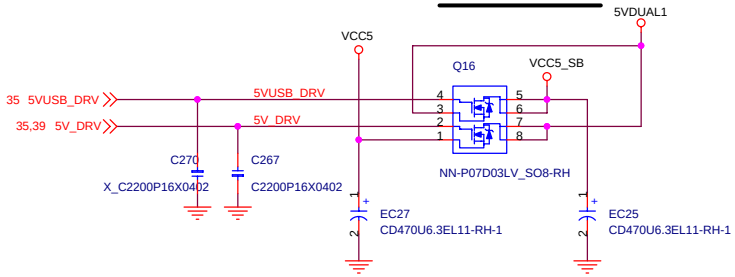
USB_FRONT

NMOS
D03-0903BDB-N03
D03-50N033B-N03
D03-60N020B-O05



USB_REAR



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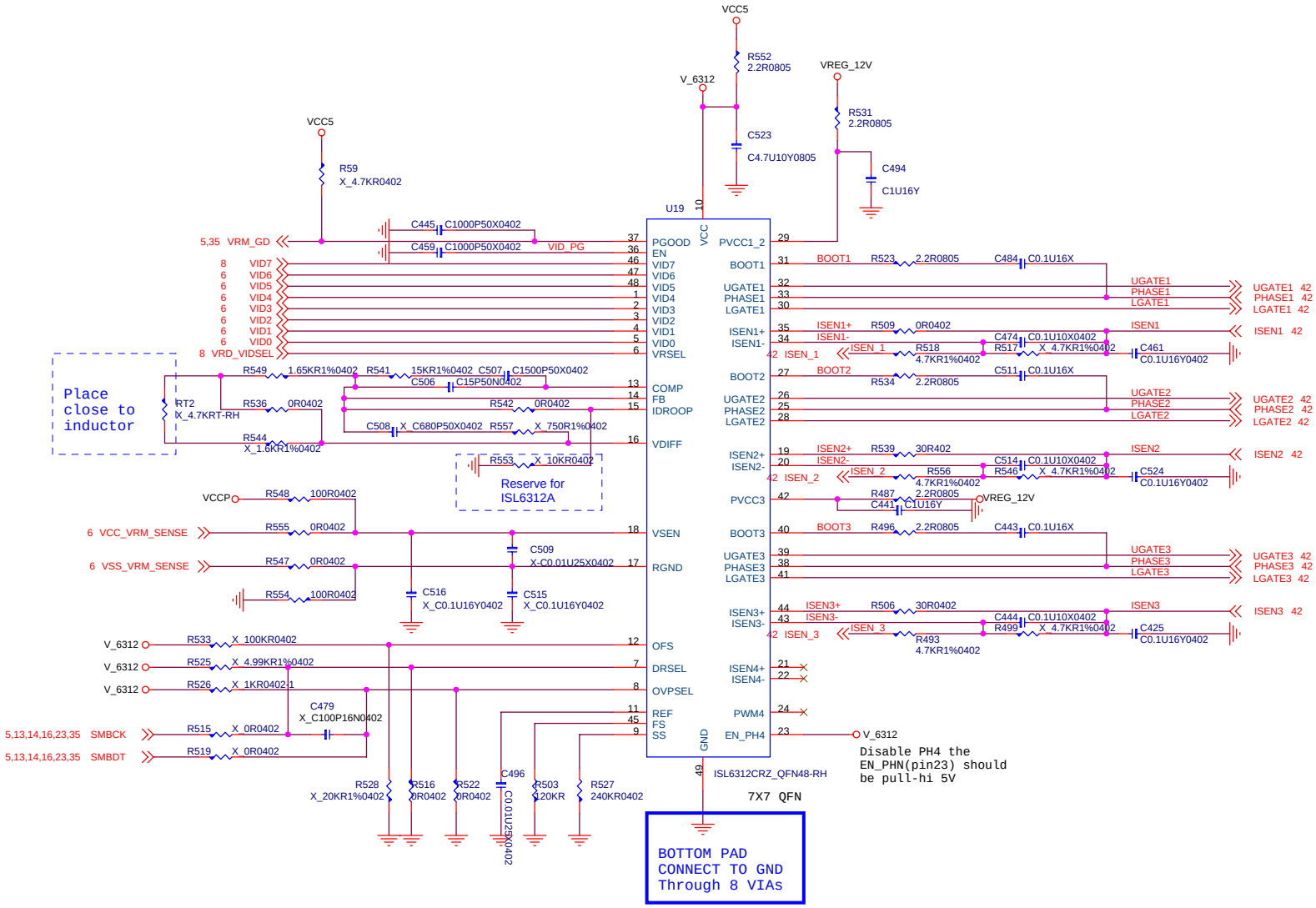

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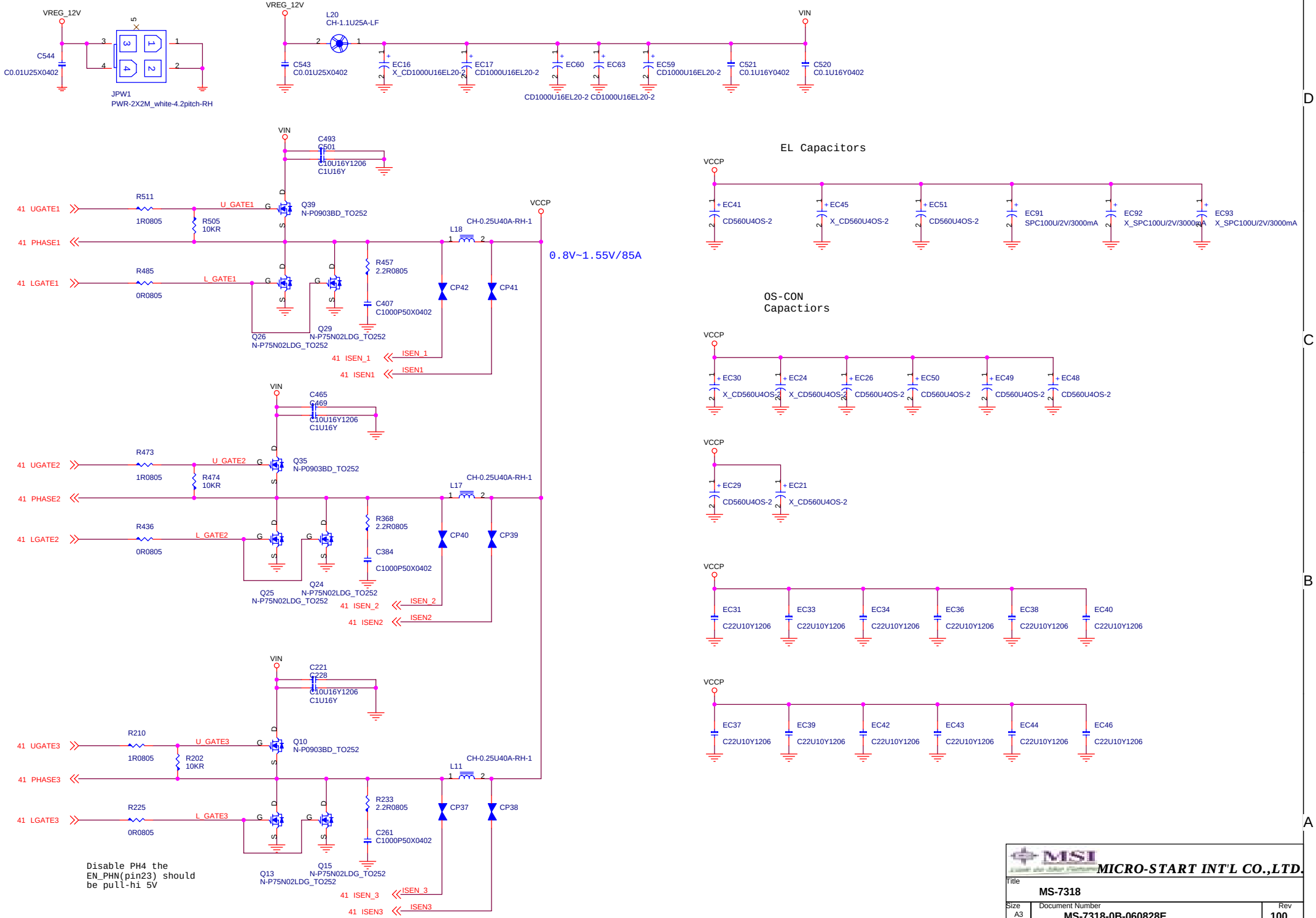

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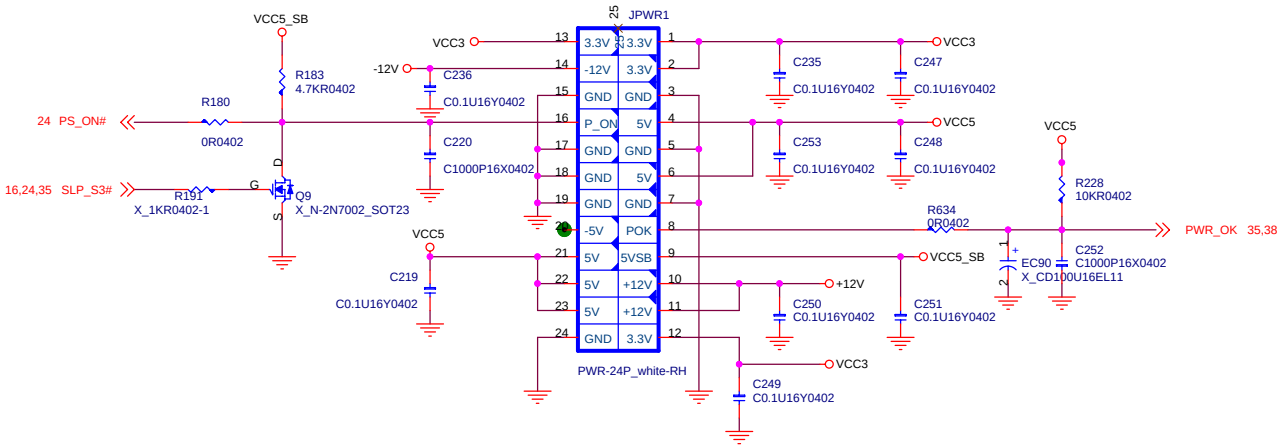
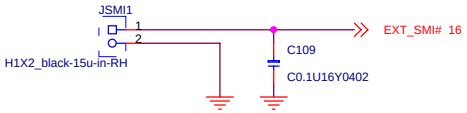
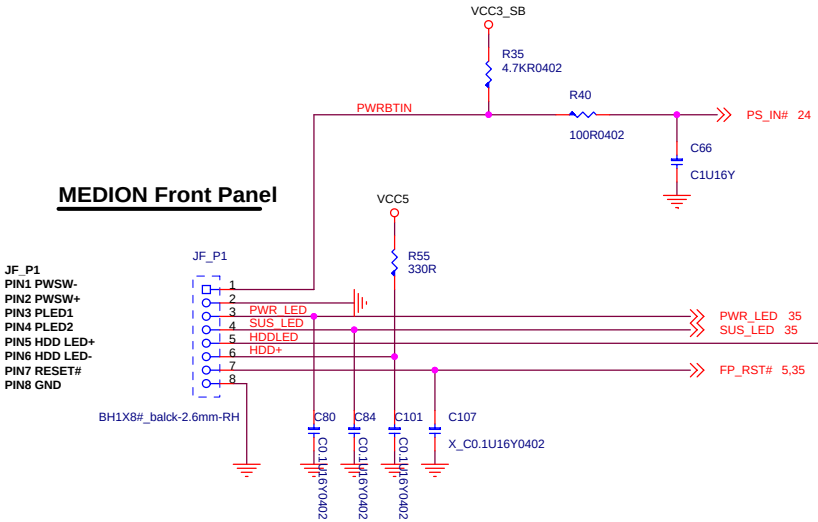
ATX Power Connector



External_SMI



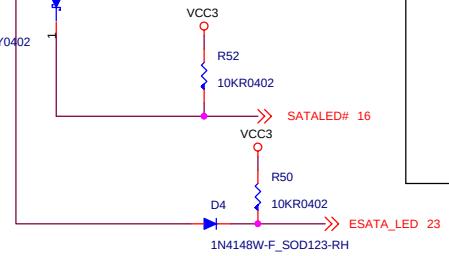
MEDION Front Panel

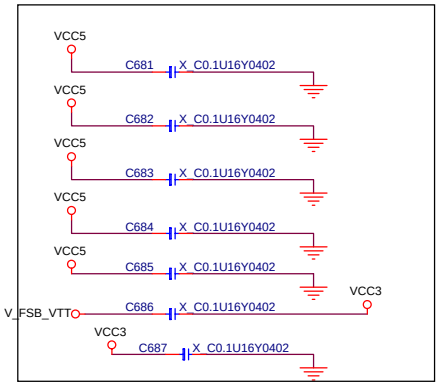


IDE LED

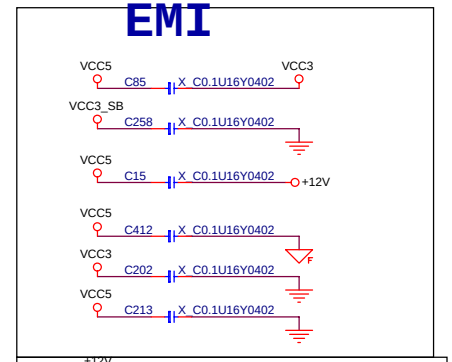
IDEACTP# 21

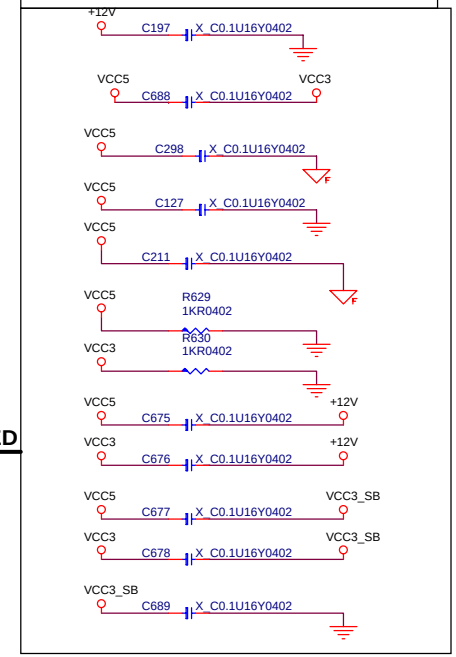
SERIAL ATA LED





EMI





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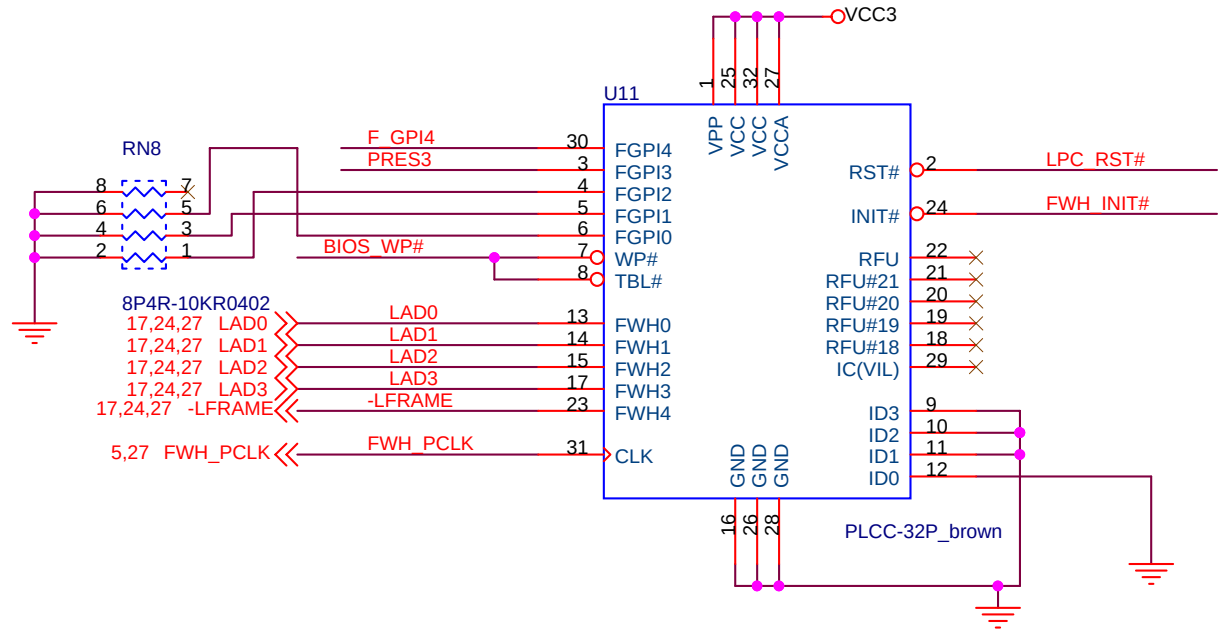
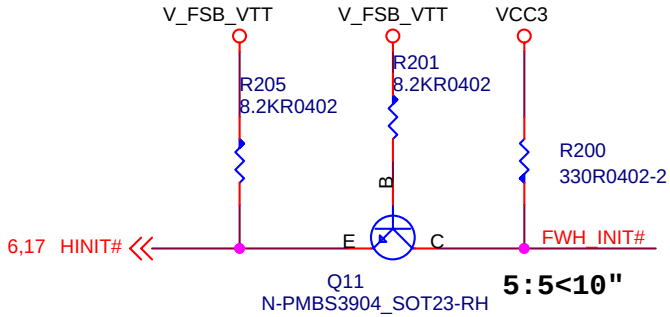
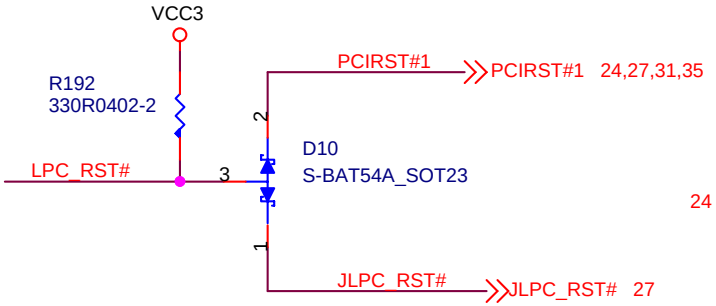
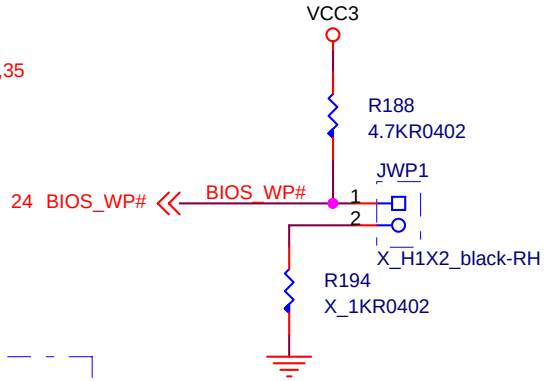
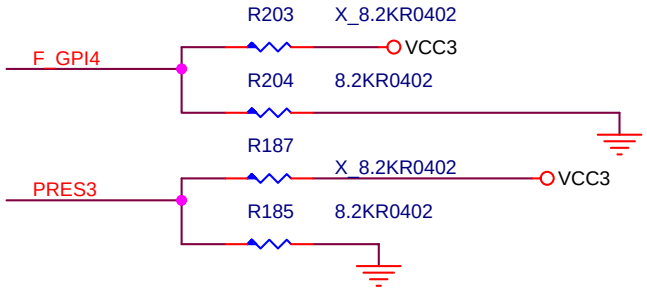


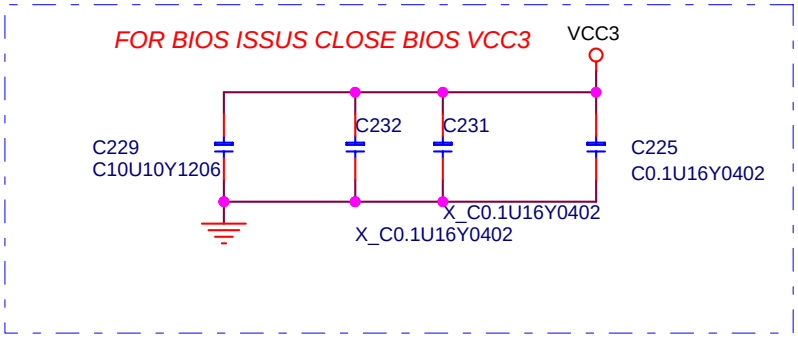
FWH INIT Signal Voltage Translation











OPEN : Un_Protected

CLOSE : Protected

Micro Star Restricted Secret

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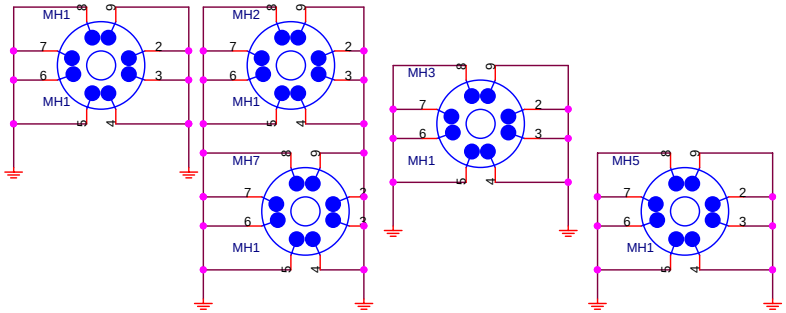
Mounting Holes



MANUAL PART

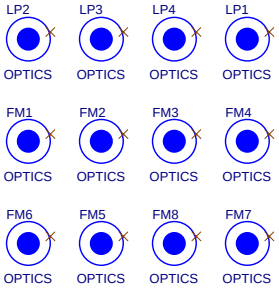
BIOS1_X1
PLCC32-SMT

PCB1
7204-1B
P30-073180B-E48
P30-0720420-G37
P30-0720420-CD7

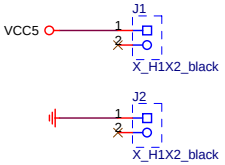
BAT1_X1
BATTERY HOLDER, 2PIN

2N7002
Top View

Optical Fiducial Marks



Simulation



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