DIGITAL DESIGN COEN 212	Ted Obuchowicz/ Asim Al-Khalili	
Time Allowed: 3:00 hrs.	Dec 13, 2017	2 pages
Answer All Questions		No materials are allowed

Question 1

1. **Design** a 3-8 decoder using NAND gates only. Mark the outputs with their corresponding binary values. (3 marks)
2. Use a 3-8 decoder plus minimal extra logic gates to implement the following functions: (3 marks)
   - **i. F1(A,B,C) = ∑ m(0,1,2)**
   - **ii. F2(A,B,C) = ∑ m(3,4,5)**
   - **iii. F3(A,B,C) = ∑ m(5,6,7)**
3. Use a 4-1 MUX plus minimal extra logic gates to implement the following function: (4 marks)

F4(A,B,C,D)=A'B' + ABC' + AB'D

Question2

1. **Design** a circuit that performs the following operations **Y= 5A** where A is an unsigned 4 bit binary number $\mathbf{A_3A_2A_1A_0}$. Give area and delay estimate of your design. [Assume all gates have equal area and delay. A full adder has 5 gates and a half adder has 2 gates]. (6 marks)
2. What size of ROM is required to implement the above multiplier? (2 marks)

Question 3

Design a Decoder that receives a BCD number and displays a **L or S** on a 7-segment display as shown in Fig. 1 below. If a BCD number is greater than OR equal TO 5 then **L** is displayed, if the number is less than 5 then **S** should be displayed. Start with a truth table and derive final output in MINIMAL SOP form. Give final circuit diagram. (8 marks)

Fig. 1