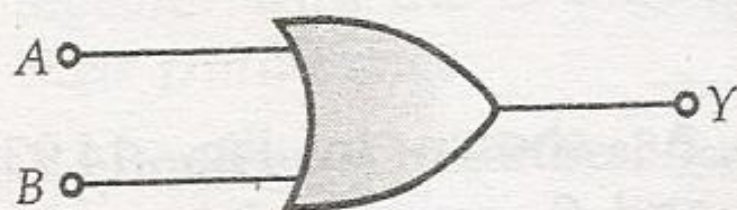**The OR gate.** *An OR gate can have any number of inputs but only one output. It gives high output (1) if either input A or B or both are high (1), otherwise the output Y is low (0).*

OR : Output is 1 if input A OR B OR both are 1

Boolean expression : $A + B = Y$

Truth Table

Logic Symbol

| Inputs		Output
A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

Fig. 14.95. The OR gate

Figure 14.95 shows the logic symbol and the truth table for an OR gate. The OR gate can be described by the *Boolean expression*

$$A + B = Y$$

which is read as '*A or B equals Y*'. Here the plus (+) sign denotes the OR function. It is obvious from the truth table of OR gate that the *output is 1 when any of the inputs is 1.*

Realisation of OR gate. As shown in Fig. 14.96, a two input OR gate can be realised by using two ideal diodes D_1 and D_2 and a resistor R. The negative terminal of the battery is grounded (*i.e.*, it is at zero volt) and corresponds to the 0 state, and the positive terminal (which is at, say 5 V) corresponds to the 1 state.
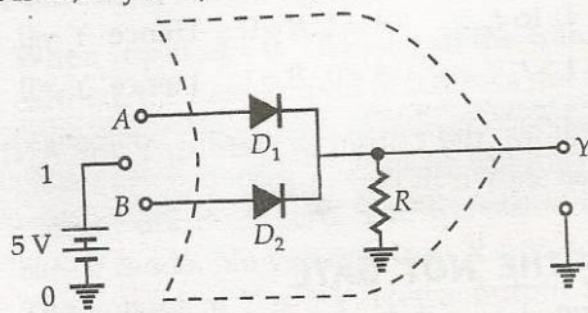

Fig. 14.96 Realisation of OR gate using two
p-n junction diodes.

The following *four* cases are possible :

1. **When $A = 0$ and $B = 0$.** Both the diodes are connected to earth (0 V). They do not conduct. Output across R is zero, *i.e.*, $Y = 0$.

2. **When $A = 0$ and $B = 1$.** D_1 is connected to earth. It does not conduct. D_2 is connected to 5 V, it gets forward biased and conducts. Voltage drop across D_2 is zero and the full voltage of 5 V appears across R. So $Y = 1$.

3. **When $A = 1$ and $B = 0$.** D_1 gets forward biased and D_2 does not conduct. Voltage drop across R is again 5 V. So $Y = 1$.

4. **When $A = 1$ and $B = 1$.** Both D_1 and D_2 get forward biased and conduct current. But D_1 and D_2 are in parallel. Voltage drop across R is still 5 V. So $Y = 1$.

Hence the circuit shown in Fig. 14.96 satisfies the truth-table of OR gate.

EXAMPLE. *Sketch the output waveform obtained from OR gate for the inputs A and B given in Fig. 14.97.*
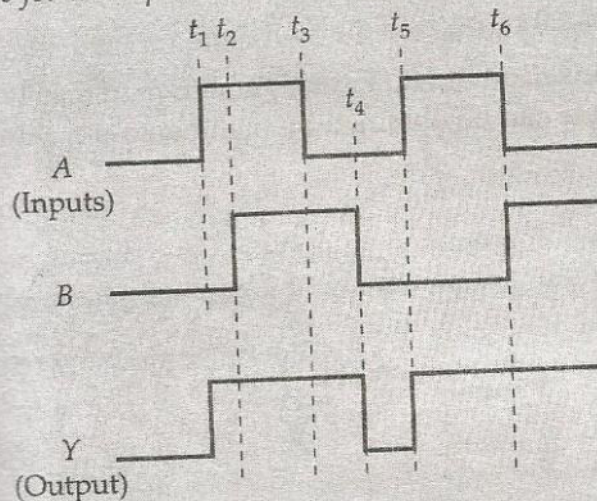
Fig. 14.97 Input and Output waveforms
for an OR gate.

Solution. The output of an OR gate is high when either A or B or both the inputs are high. When both the inputs are low, the output is low.

For $t < t_1$;	$A = 0$, $B = 0$;	Hence $Y = 0$
For t_1 to t_2 ;	$A = 1$, $B = 0$;	Hence $Y = 1$
For t_2 to t_3 ;	$A = 1$, $B = 1$;	Hence $Y = 1$
For t_3 to t_4 ;	$A = 0$, $B = 1$;	Hence $Y = 1$
For t_4 to t_5 ;	$A = 0$, $B = 0$;	Hence $Y = 0$
For $t > t_6$;	$A = 0$, $B = 1$;	Hence $Y = 1$

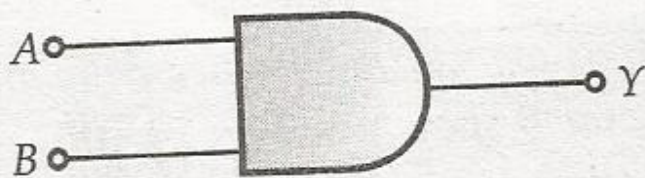Therefore the output waveform Y will be as shown in Fig. 14.97.

practice.

The AND gate. *An AND gate can have any number of inputs but only one output. It gives a high output (1) if inputs A and B are both high (1), otherwise the output Y is low (0).*

AND : Output is 1 if inputs A AND B are 1

Boolean expression : $A \cdot B = Y$

Logic Symbol

Truth Table

Inputs		Output
A	B	$Y = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

**Fig. 14.98** The AND gate.

Figure 14.98 shows the logic symbol and the truth table of an AND gate. The AND gate is described by the *Boolean expression* :

$$A \cdot B = Y$$

which is read as 'A and B equals Y'. Here the dot (.) sign represents the AND function. It is obvious from the truth table of AND gate that the *output is 1 only when both the inputs are 1.*

Realisation of AND gate. As shown in Fig. 14.99, a two input AND gate can be realised by using two ideal junction diodes D_1 and D_2. Here the resistance R is kept permanently connected to the +ve terminal of 5 V battery.
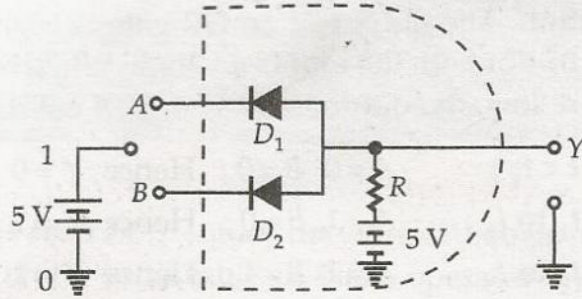
Fig. 14.99 Realisation of an AND gate.

The following *four* cases are possible :

1. **When $A = 0$ and $B = 0$.** The input terminals A and B are earthed (0 V). The two diodes get forward biased and conduct current. But both diodes are shorted. The point Y also gets earthed through the shorted diodes. Hence output $Y = 0$.

2. **When $A = 0$ and $B = 1$.** Diode D_1 is forward biased but shorted. Diode D_2 is not forward biased and does not conduct. Hence output $Y = 0$.

3. **When $A = 1$ and $B = 0$.** D_1 does not conduct. D_2 is forward biased but shorted. Hence output $Y = 0$.

4. **When $A = 1$ and $B = 1$.** Both D_1 and D_2 do not conduct as they are not forward biased. The output voltage is equal to the battery voltage of 5 V. Hence $Y = 1$.

Hence the circuit shown in Fig. 14.99 satisfies the truth table of AND gate.

EXAMPLE. *Sketch the output waveform obtained from an AND gate for the inputs A and B shown in Fig. 14.100.*
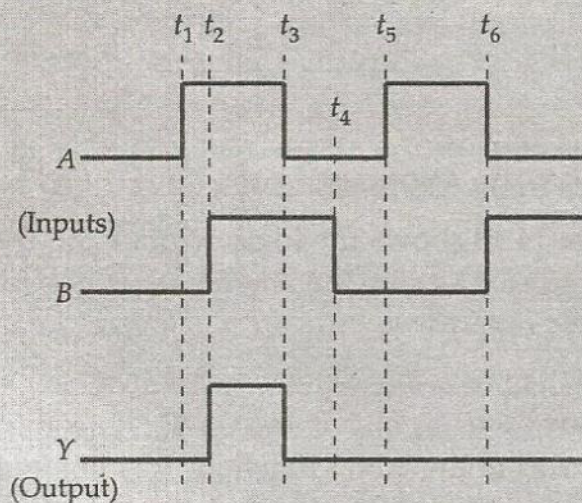
Fig. 14.100 Input and output wavefroms for an AND gate.

Solution. The output of an AND gate is high when both the inputs are high, otherwise the output is low.

For $t \le t_1$; $A = 0, B = 0$; Hence $Y = 0$

For t_1 to t_2 ; $A = 1, B = 0$; Hence $Y = 0$

For t_2 to t_3 ; $A = 1, B = 1$; Hence $Y = 1$

For t_3 to t_4 ; $A = 0, B = 1$; Hence $Y = 0$

For t_4 to t_5 ; $A = 0, B = 0$; Hence $Y = 0$

For t_5 to t_6 ; $A = 1, B = 0$; Hence $Y = 0$

For $t > t_6$; $A = 0, B = 1$; Hence $Y = 0$

Therefore, the output waveform Y for AND gate will be as shown in Fig. 14.100.

The NOT gate. *A NOT gate is the simplest gate, with one input and one output. It gives a high output (1), if the input A is low (0), and vice versa. Whatever the input, the NOT gate inverts it.*

Figure 14.101 shows the logic symbol and the truth table of NOT gate. The NOT gate is described by the *Boolean expression* :
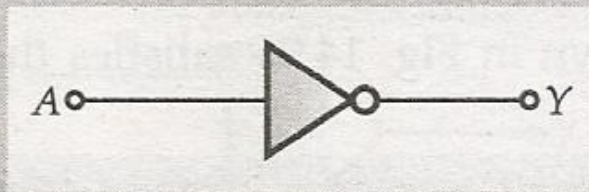
$$\overline{A} = Y$$

which is read as 'not A equals Y', i.e., Y is the negation A. This means that $Y = 0$ if $A = 1$ and $Y = 1$ if $A = 0$.

NOT : Output is high if input is low, NOT high and vice versa

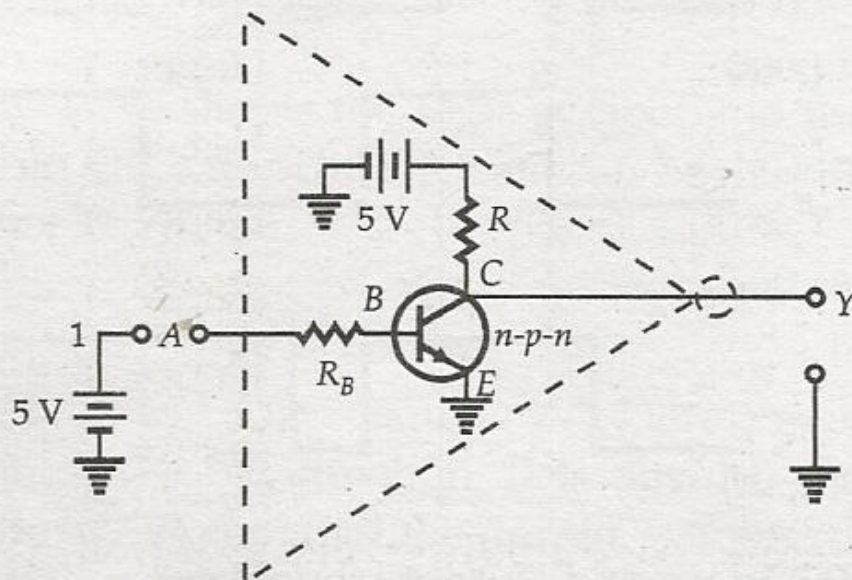**Boolean expression** : $\overline{A} = Y$

Logic Symbol

Truth Table

Input	Output
A	Y
0	1
1	0

Fig. 14.101 The NOT gate.

Realisation of NOT gate. As shown in Fig. 14.102, a NOT gate can be obtained by using an *n-p-n* transistor.

**Fig. 14.102** Realisation of a NOT gate using a transistor.

The base resistor R_B and the collector resistance R_C are so chosen that when a voltage of 5 V is applied at the base of the transistor, a large collector current flows, the voltage at Y drops and the base-collector junction is forward biased.

The following *two* cases are possible :

1. **When input $A = 0$.** The base of the transistor is earthed, the base-emitter junction is not forward biased and the collector-base junction is reverse biased. Hence the base current and the collector current are both zero. The transistor is in the *cut-off* mode. No voltage drop occurs across R_C. The voltage at Y is 5 V. Hence output $Y = 1$.

2. **When input $A = 1$.** The input terminal A is at 5 V, both emitter and collector are forward biased. A large collector current flows. The transistor is in the *saturation mode*. The voltage drop across R_C is almost 5 V. Hence output $Y = 0$.

Thus, the circuit of Fig. 14.102 satisfies the truth table of a NOT gate.

EXAMPLE. *Sketch the output waveform obtained from a NOT gate for the input A shown in Fig. 14.103.*
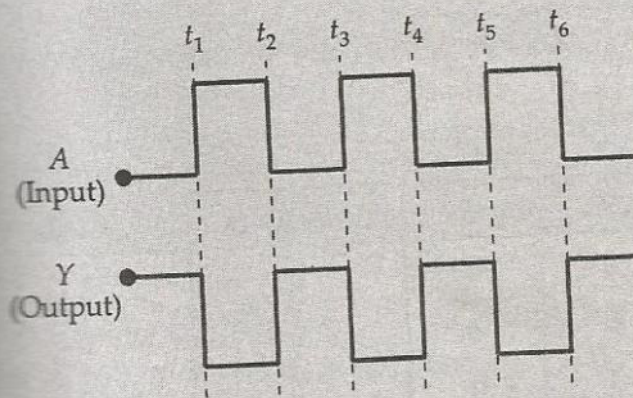
Fig. 14.103 Input and output waveforms for a NOT gate.

Solution. The output of a NOT gate is high when the input is low and vice versa.

For $t \le t_1$;	$A = 0$;	Hence $Y = 1$
For t_1 to t_2;	$A = 1$;	Hence $Y = 0$
For t_2 to t_3;	$A = 0$;	Hence $Y = 1$
For t_3 to t_4;	$A = 1$;	Hence $Y = 0$
For t_4 to t_5;	$A = 0$;	Hence $Y = 1$
For t_5 to t_6;	$A = 1$;	Hence $Y = 0$
For $t > t_6$;	$A = 0$;	Hence $Y = 1$

Therefore, the output waveform Y from NOT gate is shown in Fig. 14.103.

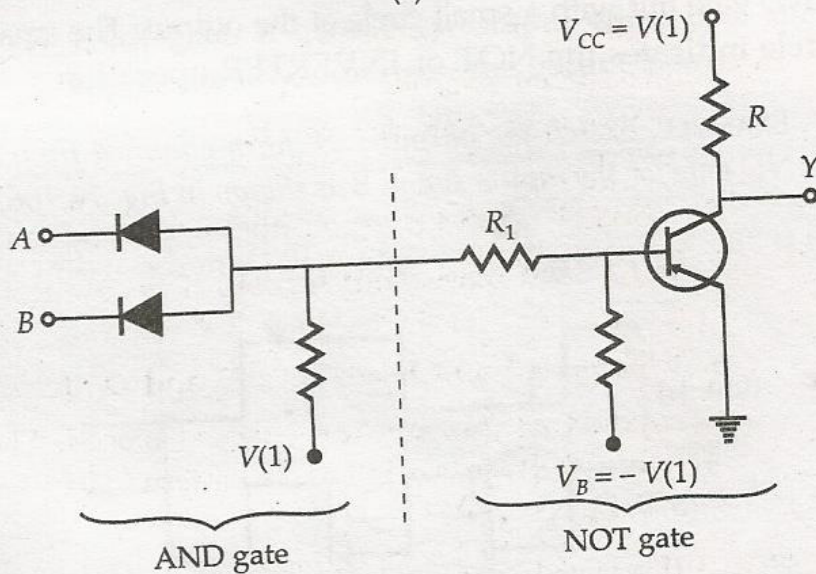**The NAND (NOT AND) gate.** A NAND gate is a combination of an AND and a NOT gate. It is obtained by connecting the output of an AND gate to the input of a NOT gate, as shown in Fig. 14.104. Its truth table can be obtained by using the truth table of AND gate and then finding the negation of its output.

(a)

(b)
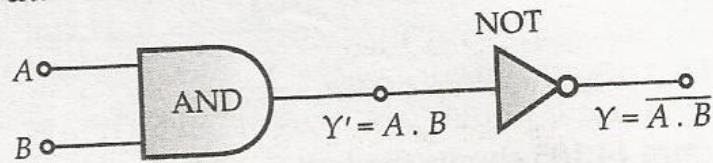
A	B	$Y' = A.B$	$Y = \overline{A.B} = \overline{Y'}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

(c)

Fig. 14.104 Realisation of a NAND gate
(a) Logic circuit (b) Practical circuit diagram
(c) Logic table.

The NAND gate is described by the *Boolean expression* :

$$\overline{A.B} = Y \quad \text{or} \quad \overline{AB} = Y$$
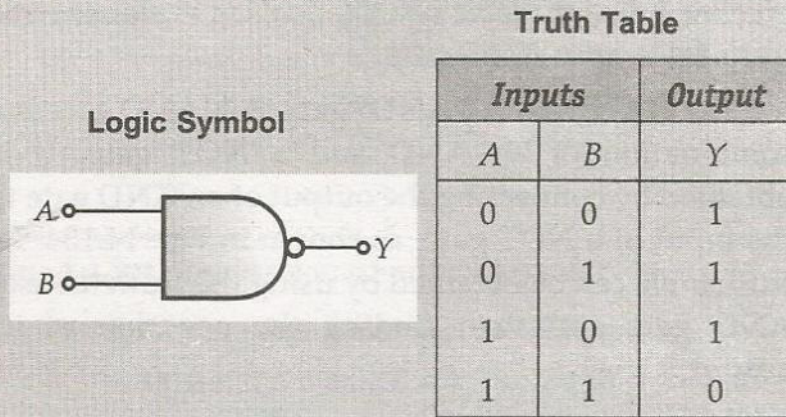
which is read as 'A AND B negated equals Y'. The output of a NAND gate is low when both the inputs are high otherwise high.

**NAND** : Output 1 if input A AND input B are NOT both 1

Boolean expression : $\overline{A.B} = Y$

Logic Symbol

Truth Table

Inputs		Output
A	*B*	*Y*
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 14.105 The NAND gate.

Figure 14.105 shows the logic symbol and the truth table of a NAND gate. The symbol is the same as for the AND gate but with a small circle at the output. The small circle indicates the NOT or INVERTER operation.

EXAMPLE. *Sketch the output waveform obtained from a NAND gate for the inputs A and B as shown in Fig. 14.106.*
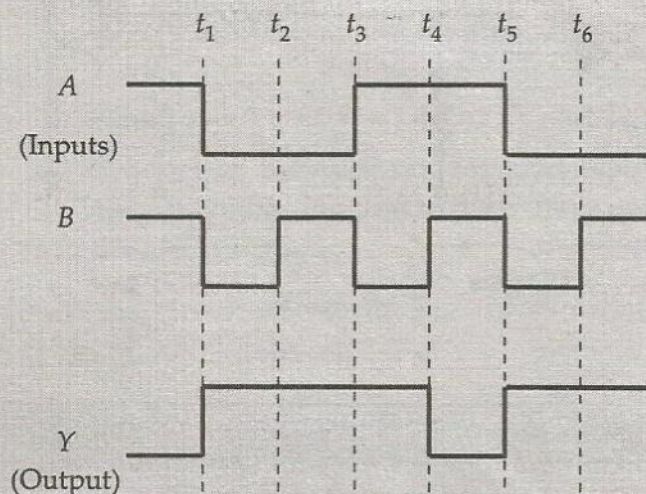
Fig. 14.106 Input and output waveforms from NAND gate.

Solution. The output of a NAND gate is low when both the inputs are high otherwise it is high.

For $t < t_1$; $\quad$ $A = 1, B = 1$; $\quad$ Hence $Y = 0$

For t_1 to t_2 ; $\quad$ $A = 0, B = 0$; Hence $Y = 1$

For t_2 to t_3 ; $\quad$ $A = 0, B = 1$; Hence $Y = 1$

For t_3 to t_4 ; $\quad$ $A = 1, B = 0$; Hence $Y = 1$

For t_4 to t_5 ; $\quad$ $A = 1, B = 1$; $\quad$ Hence $Y = 0$

For t_5 to t_6 ; $\quad$ $A = 0, B = 0$; Hence $Y = 1$

For $t > t_6$; $\quad$ $A = 0, B = 1$; Hence $Y = 1$

Therefore, the output waveform for NAND gate will be as shown in Fig. 14.106.

The NOR (NOT OR) gate. A NOR gate is a combination of an OR and a NOT gate. It is obtained by connecting the output of an OR gate to the input of a NOT gate, as shown in Fig. 14.107. Its truth table can be obtained by using the truth table of an OR gate and then finding the negation of its output.

(a)

(b)

A	B	$Y' = A + B$	$Y = \overline{A + B} = \overline{Y'}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

(c)
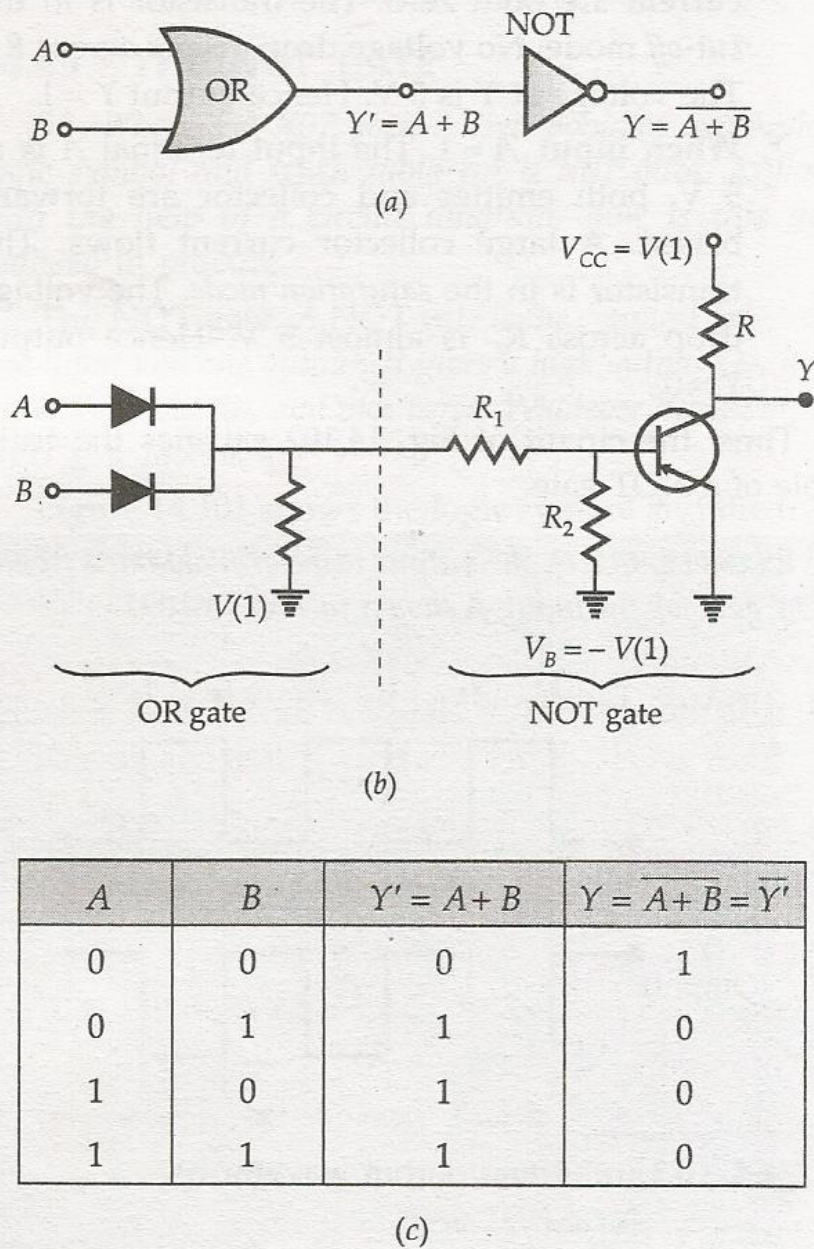
Fig. 14.107 Realisation of a NOR gate
(a) Logic circuit (b) Practical circuit diagram
(c) Logic table.

The NOR gate is described by the *Boolean expression* :

$$Y = \overline{A + B}$$

which is read as 'A OR B negated equals Y'. The output of a NOR gate is high when both the inputs are low otherwise low.

Figure 14.108 shows the logic symbol and the truth table of a NOR gate.

NOR : Output is 1 if neither input A NOR input B is 1

Boolean expression : $\overline{A+B} = Y$

Logic Symbol

Truth Table

Inputs		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Fig. 14.108. The NOR gate.

EXAMPLE. *Sketch the output waveform obtained from a NOR gate for the inputs A and B shown in Fig. 14.109.*

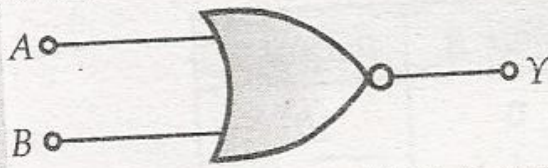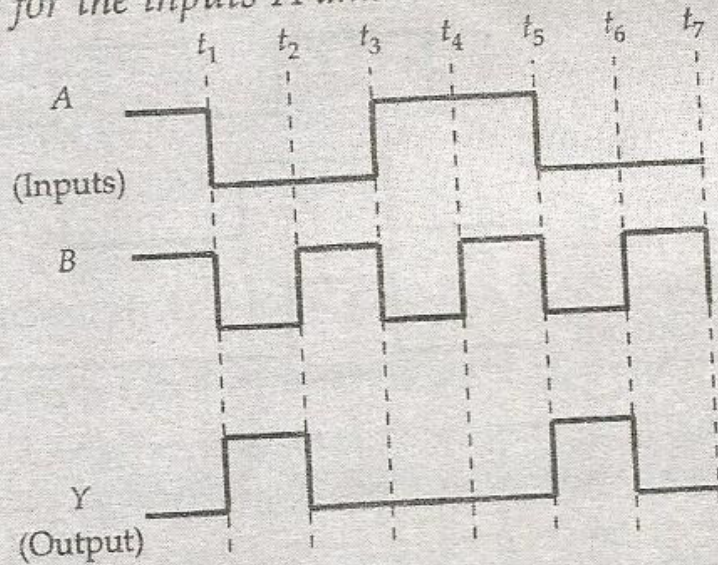

Fig. 14.109 Input and output waveforms from NOR gate.

Solution. The output of a NOR gate is high when both the inputs are low otherwise it is low.

For $t < t_1$; $A = 1, B = 1$;   Hence $Y = 0$

For t_1 to t_2 ; $A = 0, B = 0$; Hence $Y = 1$

For t_2 to t_3 ; $A = 0, B = 1$;   Hence $Y = 0$

For t_3 to t_4 ; $A = 1, B = 0$; Hence $Y = 0$

For t_4 to t_5 ; $A = 1, B = 1$;   Hence $Y = 0$

For t_5 to t_6 ; $A = 0, B = 0$; Hence $Y = 1$

For t_6 to t_7 ; $A = 0, B = 1$;   Hence $Y = 0$

AND NOR GATES AS DIGITAL

n-p-n transistor as a common emitter amplifier.

Fig. 14.74 shows the use of n-p-n transistor as a common emitter amplifier. The emitter is common to both input and output circuits. The emitter is forward biased by battery V_{BB} and the collector is reverse biased by battery V_{CC}. This decreases the resistance R_{in} of the input circuit and increases the resistance R_{out} of the output circuit. The low a.c. input signal V_i is superimposed on the forward bias V_{BE}. A load resistance R_L is connected between the collector and the d.c. supply and the amplified output is obtained between the collector and the ground.

Input
A.C. voltage
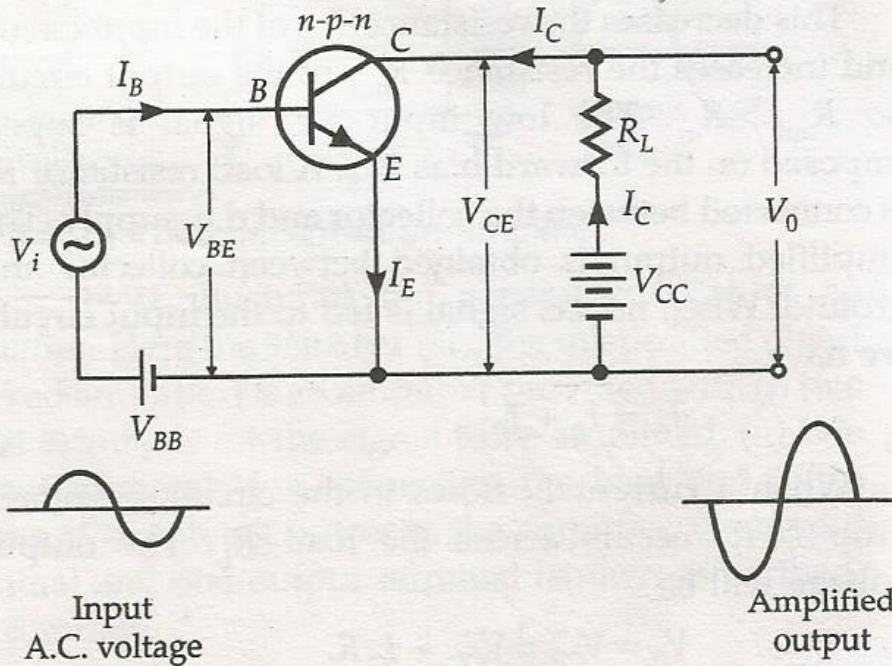
Amplified
output

Fig. 14.74 n-p-n transistor as a common emitter amplifier.

When current I_C flows in the output circuit, the potential drop across the load resistance is $I_C R_L$. Hence the output voltage is

$$V_0 = V_{CE} = V_{CC} - I_C R_L$$

When the input signal is fed to the base-emitter circuit, the base-emitter voltage changes. This changes the emitter current I_E and hence the collector current I_C. The output voltage V_0 varies in accordance with the above relation. These variations in the collector voltage appear as amplified output.

Phase relationship between input and output signals. When an a.c. signal is fed to the input circuit, its positive half cycle increases the forward bias of the circuit which, in turn, increases the emitter current and hence the collector current. The increase in collector current increases the potential drop across R_L, which

makes the output voltage V_0 less positive or more negative. So as the input signal goes through its positive half cycle, the amplified output signal goes through a negative half cycle. Similarly, as the input signal goes through its negative half cycle, the amplified output signal goes through its positive half cycle. Hence *in a common emitter amplifier, the input and output voltages are 180° out of phase or in opposite phases.*

Current, voltage and power gains of a common emitter amplifier :

a.c. current gain. *It is defined as the ratio of the small change in the collector current (ΔI_C) to the small change in base current (ΔI_B), when the collector-emitter voltage is kept constant.* It is denoted by β_{ac} or A_i. Thus

$$\beta_{ac} \quad \text{or} \quad A_i = \left[\frac{\Delta I_C}{\Delta I_B} \right]_{V_{CE} = \text{constant}}$$

d.c. current gain. *It is defined as the ratio of collector current to the base current, when collector-emitter voltage is constant.* Thus

$$\beta_{dc} = \left[\frac{I_C}{I_B} \right]_{V_{CE} = \text{constant}}$$

In the linear region of the output characteristics, β_{ac} is usually close to β_{dc}.

a.c. voltage gain. It is *defined as the ratio of small change in output voltage (ΔV_{CE}) to the small change in input voltage (ΔV_{BE}).* It is given by

$$A_v = \frac{\Delta V_{CE}}{\Delta V_{BE}}$$

But $\quad \Delta V_{BE} = R_i \cdot \Delta I_B$

where R_i is the resistance of the input or the emitter base circuit.

And $\quad \Delta V_{CE} = -R_0 \cdot \Delta I_C$

where R_0 is the resistance of the output or collector-emitter circuit (including R_L). The −ve sign indicates that the input and output voltages have a phase difference of 180° *i.e.,* if the input voltage increases, the output voltage decreases.

$$\therefore \quad A_v = -\frac{\Delta I_C}{\Delta I_B} \cdot \frac{R_{out}}{R_{in}} = -\beta_{ac} \cdot \frac{R_{out}}{R_{in}}$$

or $\quad A_v = A_i \cdot A_r$

i.e., Voltage gain = Current gain × Resistance gain.

a.c. power gain. *It is defined as the small change in output power to the small change in input power.*

$$\text{a.c. power gain} = \frac{\text{Change in output power}}{\text{Change in input power}}$$

$$= \frac{(\Delta I_C)^2 \, R_0}{(\Delta I_B)^2 \, R_i} = \beta_{ac}^2 \cdot \frac{R_0}{R_i}$$

As $\beta_{ac}^2 \gg \alpha_{ac}^2$, the a.c. power gain of a common emitter amplifier is much larger than that of a common base amplifier. It may be noted that the transistor is not generating any power. The energy for the higher a.c. power at the output is supplied by the d.c. battery.

14.39 ▼ CONCEPT OF AN AMPLIFIER

43. *What do you mean by the amplifying action of a transistor ? Why is a transistor so called ? Why is the base region of a transistor made very thin and lightly doped ? Define transconductance of a transistor.*

Amplifying action of a transistor. As the base-emitter junction of a transistor is forward biased, the depletion layer about this junction is much smaller than the depletion layer around the base-collector junction which is reverse biased. Thus the resistance R_{EB} of the emitter-base junction is much smaller than the resistance R_{BC} of the collector-base junction.

∴ Power dissipation in the emitter-base circuit,

$$P_{EB} = I_E^2 \, R_{EB}.$$

Power dissipation in the base-collector circuit,

$$P_{BC} = I_C^2 R_{BC}$$

Now $\quad I_E \simeq I_C \;$ and $\; R_{BC} \gg R_{EB}$,

∴ $$P_{BC} \gg P_{EB}$$

i.e., the power dissipated in the base-collector circuit is much higher than the power dissipated in the emitter-base circuit or *output power is much greater than the input power. This is the amplifying action of a transistor.*

Why is a transistor so called ? The collector current I_C is almost equal to the emitter current I_E. But the resistance offered by the emitter-base junction to the flow of current is small as it is forward biased. The resistance offered by the base-collector junction to the flow of current is large because this junction is reverse biased. *The current is thus transferred from a low resistance circuit to a high resistance circuit. Hence the name transistor, which is combination of the words **transfer** and **resistor.***

The base region of a transistor is very thin and lightly doped. A thin and lightly doped base region contains a smaller number of majority charge carriers. This reduces the rate of recombination of electrons and holes at the emitter-base junction. Most (95 – 99%) of the majority charge carriers, diffusing from emitter to base, reach the collector. Thus the base current is small and the collector is almost equal to the emitter current. This results in the large voltage gain and power gain of the transistor.

In a voltage amplifier, the input signal to be amplified is superposed on a steady voltage V_{EB} applied across the emitter-base junction. For a high voltage gain (the ratio of output voltage to the input voltage), the change in the collector current (ΔI_c) should be as large as possible for a given change in the emitter-base voltage (ΔV_{EB}). So we can define a figure of merit for a transistor as follows :

Transconductance. *It is defined as the ratio of the small change in the collector current to the small change in the emitter-base voltage. It is denoted by g_m.* Thus

$$g_m = \frac{\Delta I_C}{\Delta V_{BE}}$$

The transconductance is also called *transfer conductance* and has the same units of conductance (siemen or mho). The transconductance depends on the geometry, doping levels and biasing of the transistor.

44. *What is an amplifier ? Define its voltage gain.*

Concept of an amplifier. *An* **amplifier** *is a circuit (consisting of at least one transistor) which is used for increasing the voltage, current or power of alternating form.*

To amplify means to increase the size or to magnify an input signal. The output signal of an amplifier is an enlarged version of the input signal.
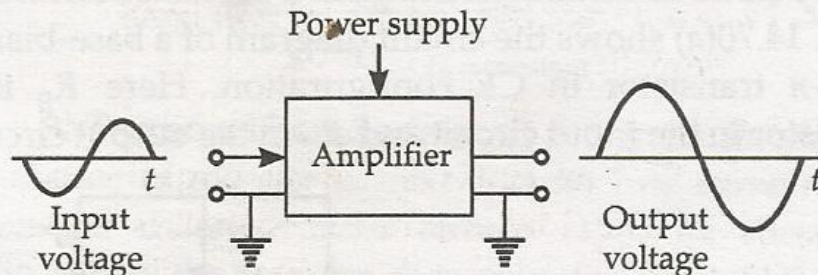
Fig. 14.71 The concept of an amplifier.

Fig. 14.71 illustrates the general concept of an amplifier. Here the *black box* (*i.e.,* the unspecified object marked amplifier) is an amplifier provided with (*i*) two input terminals for the signal to be amplified, (*ii*) two output terminals for connecting the load and (*iii*) a means of supplying power to the amplifier. One input terminal and one output terminal (shown as earthed) are common.

AC voltage gain A_v. The usefulness of an amplifier is expressed in terms of the gain of the amplifier. *The a.c. voltage gain of an amplifier is defined as the ratio of the change in the output voltage (ΔV_0) to the corresponding change in the input voltage (ΔV_i).* Thus

$$A_v = \frac{\Delta V_0}{\Delta V_i}$$

The voltage gain of an amplifier is always greater than unity. It may be noted that only the *a.c.* and not the *d.c.* components of the input and the output voltages are used to calculate the voltage gain.
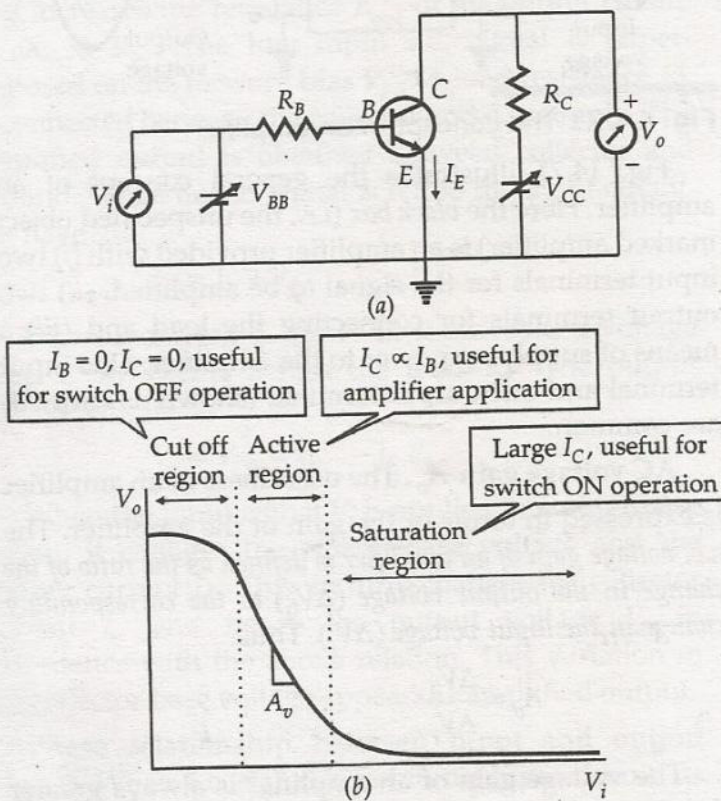
14.38 ▼ TRANSISTOR AS A SWITCH ✓

42. Explain the use of a transistor as a switch.

Transistor as a switch. Digital devices like computers perform millions of switching operations every day. Transistors can be used as such swift switches in computer circuits.

Transistors have many advantages over other electrically operated switches such as relays and reed switches.

1. Transistors are small, cheap and reliable.
2. They have no moving parts.
3. They have long life in well-designed circuits.
4. They can switch on and off millions of times a second.

Three states of a transistor. To understand the operation of a transistor as a switch, we first study the three states or conditions in which a transistor can work. Fig. 14.70(a) shows the circuit diagram of a base-biased n-p-n transistor in CE configuration. Here R_B is a resistor in the input circuit and R_C in the output circuit.

(a)

$I_B = 0$, $I_C = 0$, useful for switch OFF operation	$I_C \propto I_B$, useful for amplifier application

(b)

Fig. 14.70 (a) A base biased n-p-n transistor in CE configuration.
(b) Transfer characteristic of base-biased transistor.

Applying Krichhoff's rule to the input and output circuits separately, we get

$$V_{BB} = I_B R_B + V_{BE}$$

and

$$V_{CC} = I_C R_C + V_{CE}$$

or

$$V_{CE} = V_{CC} - I_C R_C$$

The voltage V_{BB} can be regarded as the dc input voltage V_i and V_{CE} as the dc output voltage V_0. So we can write

$$V_i = I_B R_B + V_{BE}$$

and

$$V_o = V_{CC} - I_C R_C \qquad \text{...(1)}$$

Fig. 14.70(b) shows typical output voltage (V_0) – input voltage (V_i) characteristic, called the *transfer characteristic* of the base biased transistor. It has three well-defined regions as follows :

1. *Cutoff region.* When V_i increases from zero to a low value (less than 0.6 V in case of a Si transistor), the forward bias of the emitter-base junction is insufficient to start a forward current. That is, $I_B = 0$ and hence $I_C = 0$. The transistor is said to be in the *cutoff region.* From equation (1), the output voltage $V_o = V_{CC}$.

2. *Active region.* When V_i increases slightly above 0.6 V, a current I_C flows in the output circuit and the transistor said to be in the active state. From equation (1), as the term $I_C R_C$ increases, the output voltage V_o decreases. Now as V_i increases, I_C increases almost linearly and so V_o decreases linearly till its value becomes less than 1.0 V.

3. *Saturation region.* When V_i is high *i.e.,* the emitter-base junction is heavily forward biased, a large collector current I_C flows which produces such a large potential drop across load resistance R_C that the emitter-collector junction also gets forward biased. The output voltage V_o decreases to almost zero. The transistor is said to be in the saturation state because it cannot pass any more collector current I_C.

Obviously, the transitions from cutoff state to active state and from active state to saturation state are not sharply defined because these regions of the transfer characteristic are non-linear.

Switching action of a transistor. A transistor can be used as a switch if it is operated in its cutoff and saturation states only. A switch circuit is designed in such a manner that the transistor does not remain in the active state. As long as the input voltage is low and unable to forward-bias the transistor, the output voltage V_o (at V_{CC}) is high. If V_i is high enough to drive the transistor into saturation, then V_o is low, nearly zero. When the transistor is not conducting, it is said to be *switched off* and when it is driven into saturation, it is said to be *switched on.* So if we define low (0) and high (1) states as below and above certain voltage levels corresponding to cutoff and saturation of the transistor, then a low input switches the transistor off and a high input switches it on. Alternatively, we can say that a low input to the transistor gives a high output and high input gives a low output.

Action of _n-p-n_ transistor. The _n_-type emitter of _n-p-n_ transistor is forward biased by connecting it to the −ve terminal of battery V_{EB} and the _n_-type collector is reverse biased by connecting it to the +ve terminal of battery V_{CB}, as shown in Fig. 14.63.

The forward bias of the emitter-base circuit repels the electrons of emitter towards the base, setting up emitter current I_E. As the base is very thin and lightly doped, a very few electrons (< 5%) from the emitter combine with the holes of base, giving rise to base
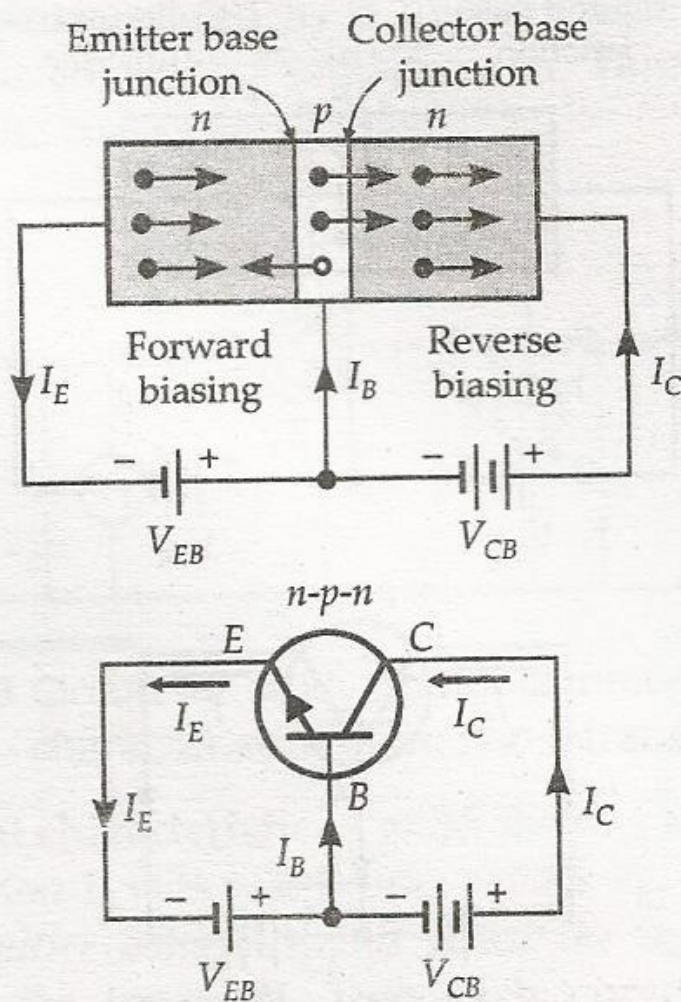
Fig. 14.63 Action of *n-p-n* transistor and its biasing.

current I_B and the remaining electrons ($>95\%$) are pulled by the collector which is at high positive potential. The electrons are finally collected by the +ve terminal of battery V_{CB}, giving rise to collector current I_C.

As soon as an electron from the emitter combines with a hole in the base region, an electron leaves the negative terminal of the battery V_{EB} and at the same time the positive terminal of battery V_{EB} receives an electron from the base. This sets a base current I_B. Similarly, corresponding to each electron that goes from collector to positive terminal of V_{CB}, an electron enters the emitter from negative terminal of V_{EB}. Hence

Emitter current = Base current + Collector current

or $\qquad I_E = I_B + I_C \qquad\qquad [I_B \ll I_C]$

Here I_B is a small fraction of I_C depending on the shape of transistor, thickness of base, doping levels, bias voltages, etc.

Action of p-n-p transistor. The p-type emitter of p-n-p transistor is forward biased by connecting it to the +ve terminal of battery V_{EB} and the p-type collector is reverse biased by connecting it to the −ve terminal of battery V_{CB} as shown in Fig. 14.64.

The forward bias of the emitter-base circuit repels the holes of emitter towards the base and electrons of base towards the emitter. As the base is very thin and lightly doped, most of the holes (> 95%) entering it pass on to collector while a very few of them (< 5%) recombine with the electrons of the base region.
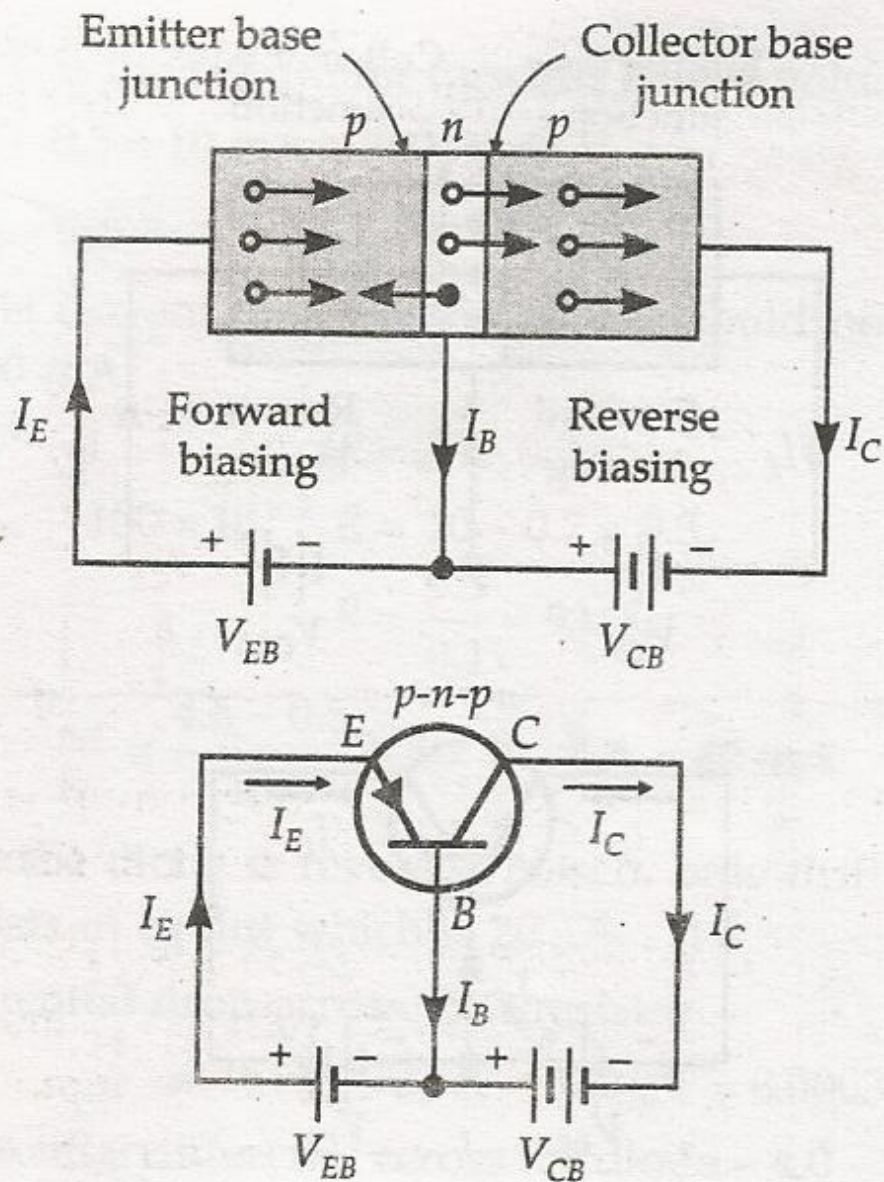
Fig. 14.64 Action of p–n–p transistor and its biasing.

As soon as a hole combines with an electron, an electron from the negative terminal of the battery V_{EB} enters the base. This sets up a small base current I_B. Each hole entering the collector region combines with an electron from the negative terminal of the battery V_{CB} and gets neutralised. This creates collector current I_C. Both the base current I_B and collector current I_C combine to form emitter current I_E.

$$\therefore \quad I_E = I_B + I_C$$

Thus inside the p-n-p transistor, the current conduction is due to holes while electrons are the charge carriers in the external circuit.

14.36 ▼ CURRENT GAINS IN A TRANSISTOR

40. *Define the two current gains of a transistor and deduce a relation between them.*

Current gains in a transistor. Usually *two* types of current gains are defined for a transistor :

1. Common base current amplification factor or a.c. current gain α. *It is defined as the ratio of the small change in the collector current to the small change in the emitter current when the collector-base voltage is kept constant.* Thus

$$\alpha = \left[\frac{\Delta I_C}{\Delta I_E} \right]_{V_{CB} = \text{constant}}$$

2. Common emitter current amplification factor or a.c. current gain β. *It is defined as the ratio of the small change in the collector current to the small change in the base current when the collector-emitter voltage is kept constant.* Thus

$$\beta = \left[\frac{\Delta I_C}{\Delta I_B} \right]_{V_{CE} = \text{constant}}$$

Relation between α and β. For both n-p-n and p-n-p transistors, we have

$$I_E = I_B + I_C$$

For small changes, we can write

$$\Delta I_E = \Delta I_B + \Delta I_C$$

Dividing both sides by ΔI_C,

$$\frac{\Delta I_E}{\Delta I_C} = \frac{\Delta I_B}{\Delta I_C} + 1$$

or

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1 \qquad \left[\because \frac{\Delta I_C}{\Delta I_E} = \alpha \; ; \; \frac{\Delta I_C}{\Delta I_B} = \beta \right]$$

or

$$\alpha = \frac{\beta}{1+\beta}$$

and

$$\beta = \frac{\alpha}{1-\alpha}$$

As the value of I_B is about $1-5\%$ of I_E or I_C is $95-99\%$ of I_E, α is about 0.95 to 0.99 and β is about 20 to 100. The CE configuration is frequently used as it gives high current gain as well as voltage gain.

Note 1. α and β are independent of current if the emitter-base junction is forward biased and the collector-base junction is reverse biased.

2. The above definitions of α and β do not hold when both the junctions of a transistor are forward biased or reverse biased.

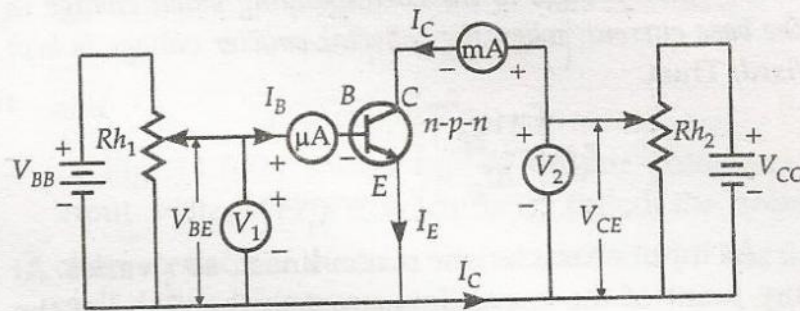## 14.37 ▼ COMMON EMITTER CHARACTERISTICS

41. *Draw a circuit diagram for an n-p-n transistor in common emitter configuration to study its (i) input, (ii) output and (iii) transfer characteristics. Draw approximate shape of these curves and give their important features. How will you use these characteristics to obtain (i) input resistance, (ii) output resistance and (iii) current amplification factor ?*

Common emitter characteristics. The common-emitter characteristics are the graphs drawn between appropriate voltages and currents for a transistor when its emitter is taken as the common terminal and grounded (zero potential), base is the input terminal and collector is the output terminal.

Fig. 14.66 shows the circuit diagram for studying the common emitter characteristics of an n-p-n transistor. The emitter-base junction is forward biased by means of battery V_{BB} through rheostat Rh_1. The emitter-collector circuit is reverse biased by means of battery V_{CC} through rheostat Rh_2. The base-emitter voltage V_{BE} and the collector-emitter-voltage V_{CE} are measured by high resistance voltmeters. The base

current I_B is measured by a microammeter and the collector current I_C by a milliammeter. Three types of characteristic curves are studied.

Fig. 14.66 Circuit for studying the common emitter characteristics of an *n–p–n* transistor.

1. Input characteristic. *A graph showing the variation of base current I_B with base-emitter voltage V_{BE} at constant collector-emitter voltage V_{CE} is called the input characteristic of the transistor.* Two such curves for two different collector-emitter voltages have been plotted in Fig. 14.67.
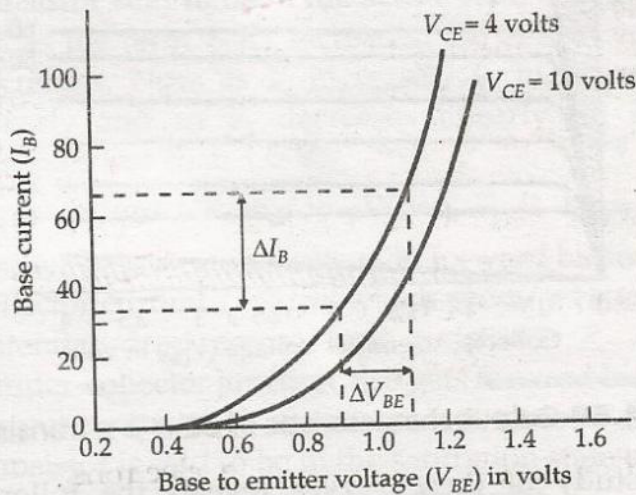
Fig. 14.67 Input characteristics of CE *n-p-n* transistor.

A study of the these curves reveals the following facts :

(i) As long as V_{BE} is less than the barrier voltage, the base current I_B is small as in the case of forward biased diode.

(ii) When the base-emitter voltage V_{BE} exceeds the barrier voltage, the base current I_B increases sharply with a small increase in V_{BE} as in the case of a forward biased diode.

(iii) The value of I_B is much smaller than that in a normal diode, more than 95% majority emitter carriers (electrons in *n-p-n* and holes in *p-n-p* transistor) go to the collector to constitute the collector current I_C.

Since the increase in V_{CE} appears as the increase in V_{CB}, its effect on I_B is negligible. As a result, input characteristics for various values of V_{CE} give almost identical curves. Hence, *it is enough to determine only one input characteristic.*

The input resistance r_i of the transistor in CE configuration is defined as the ratio of the small change in base-emitter voltage to the corresponding small change in the base current, when the collector-emitter voltage is kept fixed. Thus

$$r_i = \left[\frac{\Delta V_{BE}}{\Delta I_B}\right]_{V_{CE} = \text{constant}}$$

As input characteristic is non-linear, so r_i varies. At any point of the curve, r_i is equal to the slope of the tangent to the curve.

2. Output characteristic. *A graph showing the variation of collector current I_C with collector-emitter voltage V_{CE} at constant base-current I_B is called the output characteristic of the transistor.* Fig. 14.68 shows such curves for different values of I_B.
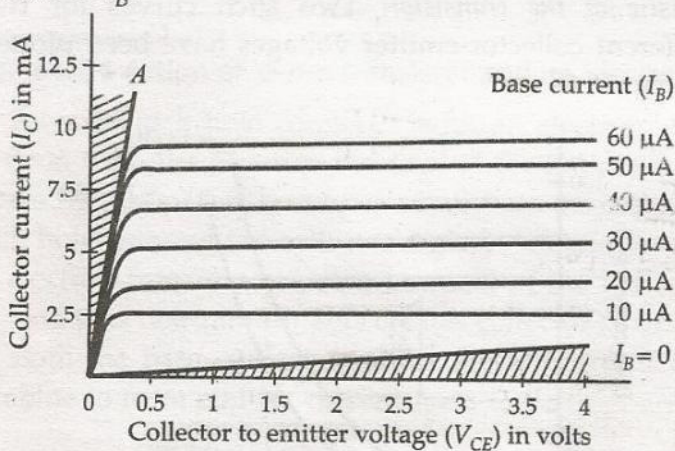
Fig. 14.68 Output characteristic of *CE n-p-n* transistor.

A study of these curves reveals the following features :

(i) When the voltage V_{CE} increases from 0 to about 0.5 V, the collector current I_C increases rapidly. The value of V_{CE} upto which I_C increases rapidly is called *knee voltage.*

(ii) Once the voltage V_{CE} exceeds the voltage V_{BE} (so that the collector-base junction is reverse biased), the output current I_C varies *very slowly* but *linearly* with V_{CE} for a given base current I_B, i.e., beyond the knee voltage the output resistance of the transistor is high.

(iii) Larger the value of I_B, larger is the value of I_C for a given V_{CE}.

Three regions of the output characteristic :

(a) The shaded region towards the left of line *OA* is called *saturation region* and the line *OA* is called *saturation line.* Here $V_{CE} < V_{BE}$. Both the junctions are forward biased. Here I_C does not depend on the input current I_B.

(b) The shaded region lying below the curve for $I_B = 0$ is called *cut-off region.* In this region, both the junctions are reverse biased. Here $I_C = 0$. In the shaded regions, the transistor works as *switch;* it turns over rapidly from OFF state for which $I_C = 0$ (*cut-off*) to the ON state for which I_C is maximum (*saturation state*).

(c) The non-shaded central region of the output characteristic is called *active region.* In this region, the emitter-base junction is forward biased and the collector-base junction is reverse biased. A transistor works as an *audio amplifier* in this region.

The **output resistance** r_0 of a transistor in CE configuration is defined as the ratio of the small change in the collector-emitter voltage to the corresponding change in the collector current when the base current is kept constant. Thus

$$r_0 = \left[\frac{\Delta V_{CE}}{\Delta I_C}\right]_{I_B = \text{constant}}$$

3. Transfer characteristic. *It is a graph showing the variation of collector current I_C with base current I_B at constant collector-emitter voltage V_{CE}.* As shown in Fig. 14.69, the transfer characteristic of a transistor is almost a straight line.
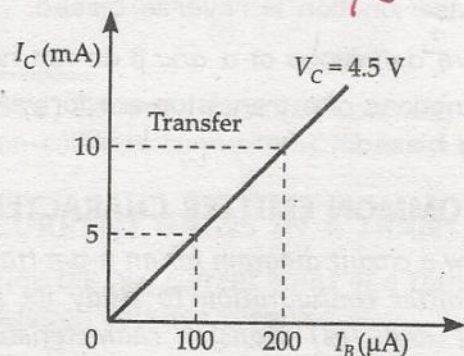

Fig. 14.69 Transfer characteristic of *CE n-p-n* transistor.

Current amplification factor (β). *It is defined as the ratio of the change in collector current to the small change in base current at constant collector-emitter voltage (V_{CE}) when the transistor is in the active state.*

$$\beta_{ac} = \left[\frac{\Delta I_C}{\Delta I_B}\right]_{V_{CE} = \text{constant}}$$

This is also known as small *signal current gain* and its value is very large. The direct ratio of I_C and I_B gives the *dc current gain* (β_{dc}) of the transistor. Hence,

$$\beta_{dc} = \frac{I_C}{I_B}$$

Since I_C increases with I_B almost linearly and $I_C = 0$ when $I_B = 0$, *the values of both β_{ac} and β_{dc} are nearly equal.*
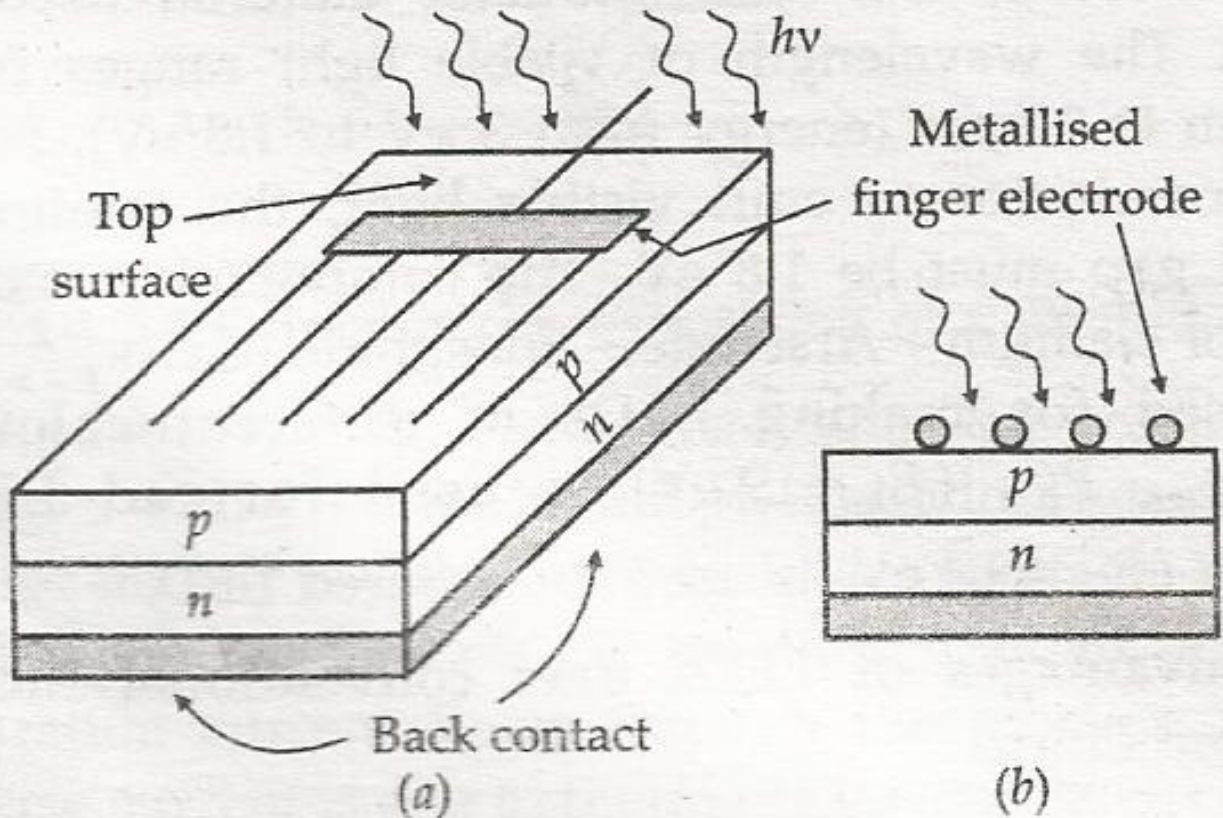
14.30 ▼ SOLAR CELL

34. *What is a solar cell ? Briefly describe the construction and working of a typical p-n junction solar cell. Give its V-I characteristic. Name the materials commonly used to prepare solar cells.*

Solar cell. *It is a junction diode which converts solar energy into electricity and is based on photovoltaic effect* (generation of voltage due to bombardment of light photons).

Construction. It consists of a p-n junction made from Si or GaAs. Here a thin layer of p-type is grown (by diffusion of a suitable acceptor impurity or by vapour deposition) on an n-type semiconductor. The

Fig. 14.40 (a) A typical p-n junction solar cell.
(b) Sectional view of the solar cell.

top of the p-layer is provided with few finger electrodes. This leaves open enough space for the light to reach the thin p-layer and hence the underlying p-n junction. The bottom of the n-layer is provided with a current collecting electrode.

Working. When light photons (with energy $hv > E_g$) reach the junction, they excite electrons from the valence band to conduction band, leaving behind equal number of holes in the valence band. These electron-hole pairs generated in the depletion region move in opposite directions due to the barrier field. Photo-generated electrons move towards n-sides and holes towards p-side. The collection of these charge carriers makes p-side a positive electrode and n-side a negative electrode. Hence *photo-voltage* is set up across the junction. When a load resistance R_L is connected in the external circuit, a photo-current I_L flows, as shown in Fig. 14.41(a). This current is proportional to the intensity of illumination.
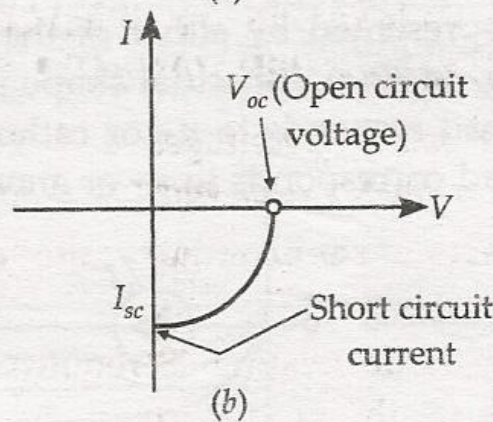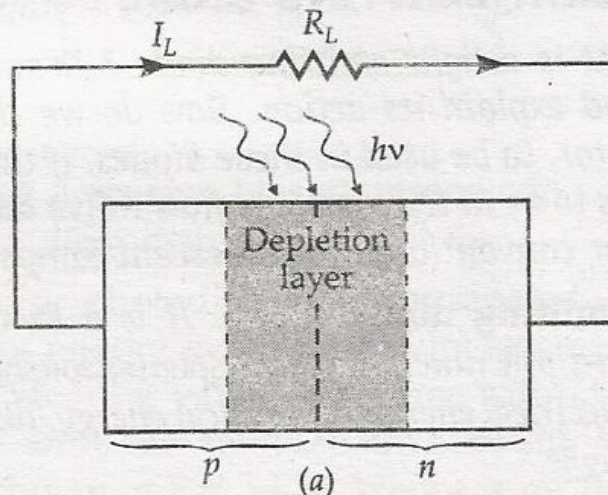
Fig. 14.41 (a) Photo-current through an illuminated p-n junction. (b) V-I characteristic of a solar cell.

Fig. 14.41(b) shows the V-I characteristic of a solar cell. The open circuit voltage V_{OC} depends on the illumination. Hence the output power of a solar cell depends on the intensity of incident sunlight.

33. *What is a light emitting diode ? Draw a circuit diagram and explain its action. How do we choose the semiconductor, to be used in these diodes, if the emitted radiation, is to be in the visible region ? Give advantages of LEDs over conventional incandescent lamps.*

Light emitting diode (LED). *It is a heavily-doped forward-biased p-n junction which spontaneously converts the biasing electrical energy into optical energy, like infrared and visible light.*

LED is represented by either of the two symbols shown in Fig. 14.37(a). Its actual shape is also shown, the shorter lead responds to n - or cathode side while the longer lead corresponds to p - or anode side.
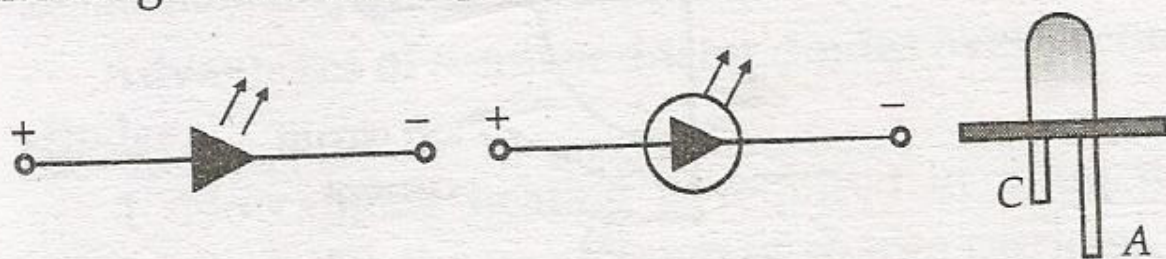
Fig. 14.37(a) LED symbol and shape.

A p-n junction made from a translucent semi-conductor like gallium arsenide or indium phosphide is provided with metallised contacts, as shown in Fig. 14.37(b). When it is forward biased through a series resistance R, light photons are emitted from the non-metallised surface of the n-region. The series resistance R limits the current through the LED and hence controls the intensity of light emitted by it.
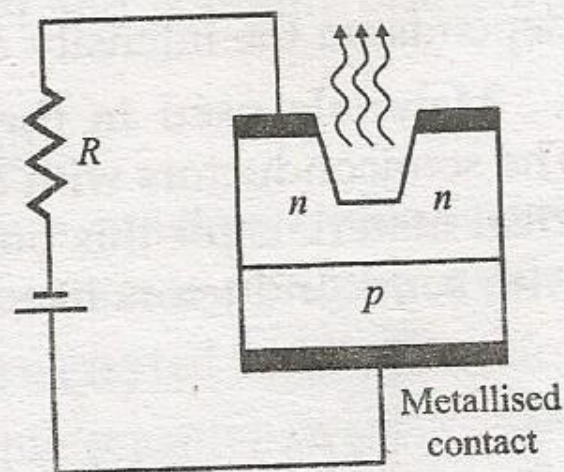

Fig. 14.37(b) A forward biased LED.

When the p-n junction is forward biased, electrons are sent from n-region → p-region (where they are minority carriers) and holes are sent from p-region → n-region (where they are minority carriers). Near the junction, the concentration of minority carriers increases as compared to the equilibrium concentration (i.e., when there is no bias). On either side near junction, the excess minority carriers combine with the majority carriers. On recombination, the energy is released in the form of photons. Photons with energy equal to or slightly less than the band gap are emitted. When the forward bias of the diode is small, the intensity of emitted light is small. As the forward current increases, intensity of light increases and reaches a maximum. Further increase in forward current decreases the light intensity. LEDs are biased such that the light emitting efficiency is maximum.

The general shape of the I-V characteristics of an LED is similar to that of a normal p-n junction diode, as shown in Fig. 14.38. However, the barrier potentials are much higher and slightly different for each colour.
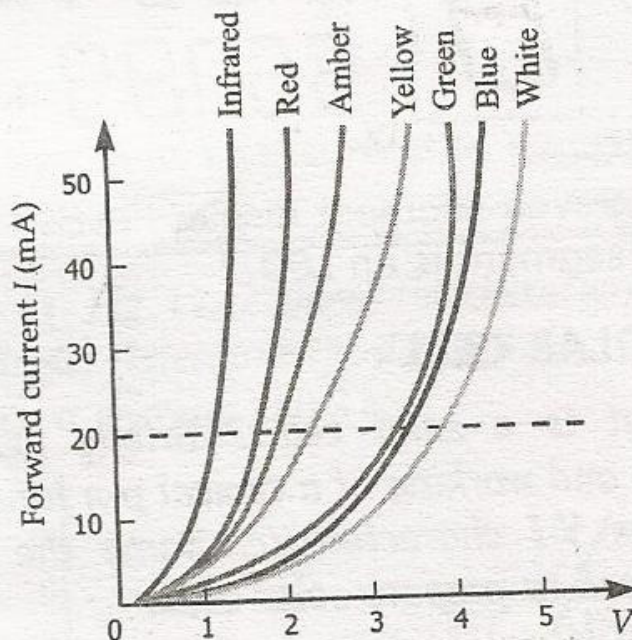
Fig. 14.38 I-V characteristics of LED.

Two important features of LEDs are :

1. The colour of light emitted by an LED depends on its band-gap energy.

2. The intensity of light emitted is determined by the forward current conducted by the p-n junction.

14.28 ▼ PHOTODIODES

32. *What is a photodiode ? Explain its working principle. Why is a photodiode operated in reverse bias ? Give some important uses of photodiodes.*

Photodiode. *A photodiode is a p-n junction fabricated from a photosensitive semiconductor and provided with a transparent window so as allow light to fall on its junction. Its symbolic representation is shown in Fig. 14.34.*
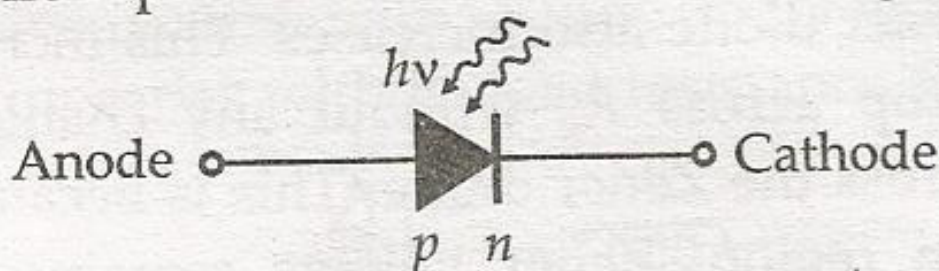

Fig. 14.34 Symbolic representation of a photodiode.

As shown in Fig. 14.35, a resistance R is connected in series with a reverse biased photodiode. The voltage is kept slightly less than the breakdown voltage. When no light is incident on the junction, a small reverse saturation current flows through the junction. This reverse current is due to thermally generated electron-hole pairs and is called *dark current*.

When the photodiode is illuminated with light photons of energy $h\nu$ greater than the energy gap E_g of the semiconductor, additional electron-hole pairs are generated due to the absorption of photons. This generation of photogenerated charge carriers occurs in or near the depletion region. Due to the junction field, electrons get collected on n-side and holes on the p-side setting up an emf. This sends a current through the load. In a reverse biased photodiode, we can easily observe the change in photocurrent with the change in radiation intensity. Hence a photodiode can be used to detect optical signals.
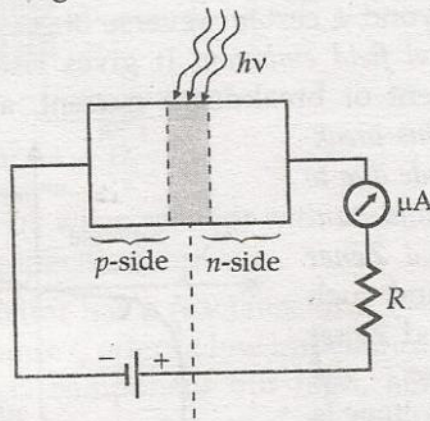
Fig. 14.35 A reverse biased photodiode Illuminated with light.

When a photodiode is illuminated with light photons of energy $h\nu > E_g$, and increasing intensities I_1, I_2, I_3, etc., the value of reverse saturation current increases with the increase in intensity of incident light, as shown in Fig. 14.36. Hence, a measurement of the change in the reverse saturation current on illumination can give the values of light intensity.
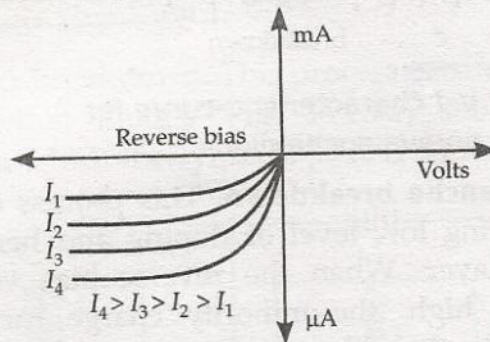
Fig. 14.36 Reverse bias currents through a photodiode when illuminated with different intensities.

A photodiode is preferably operated in reverse bias condition. Consider an n-type semiconductor. Its majority carrier (electron) density is much larger than the minority hole density i.e., $n \gg p$. When illuminated with light, both types of carriers increase equally in number.

$$n' = n + \Delta n ; \qquad p' = p + \Delta p$$

Now $n \gg p$ and $\Delta n = \Delta p$

$$\therefore \quad \frac{\Delta n}{n} \ll \frac{\Delta p}{p}$$

14.25 ▼ CAUSE OF REVERSE BREAKDOWN OF A JUNCTION DIODE

29. *Explain the two processes which are responsible for the breakdown of a junction diode.*

Cause of reverse breakdown of a junction diode. The breakdown of a junction diode may occur through two different processes :

1. Zener breakdown. This process occurs in *heavily doped* junction diodes. Fig. 14.28(a) shows a p-n junction in which the symbols p^+ and n^+ indicate that
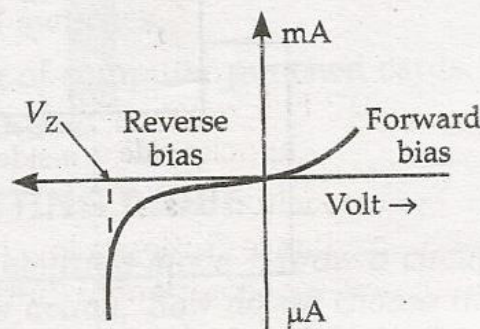

Narrow depletion layer
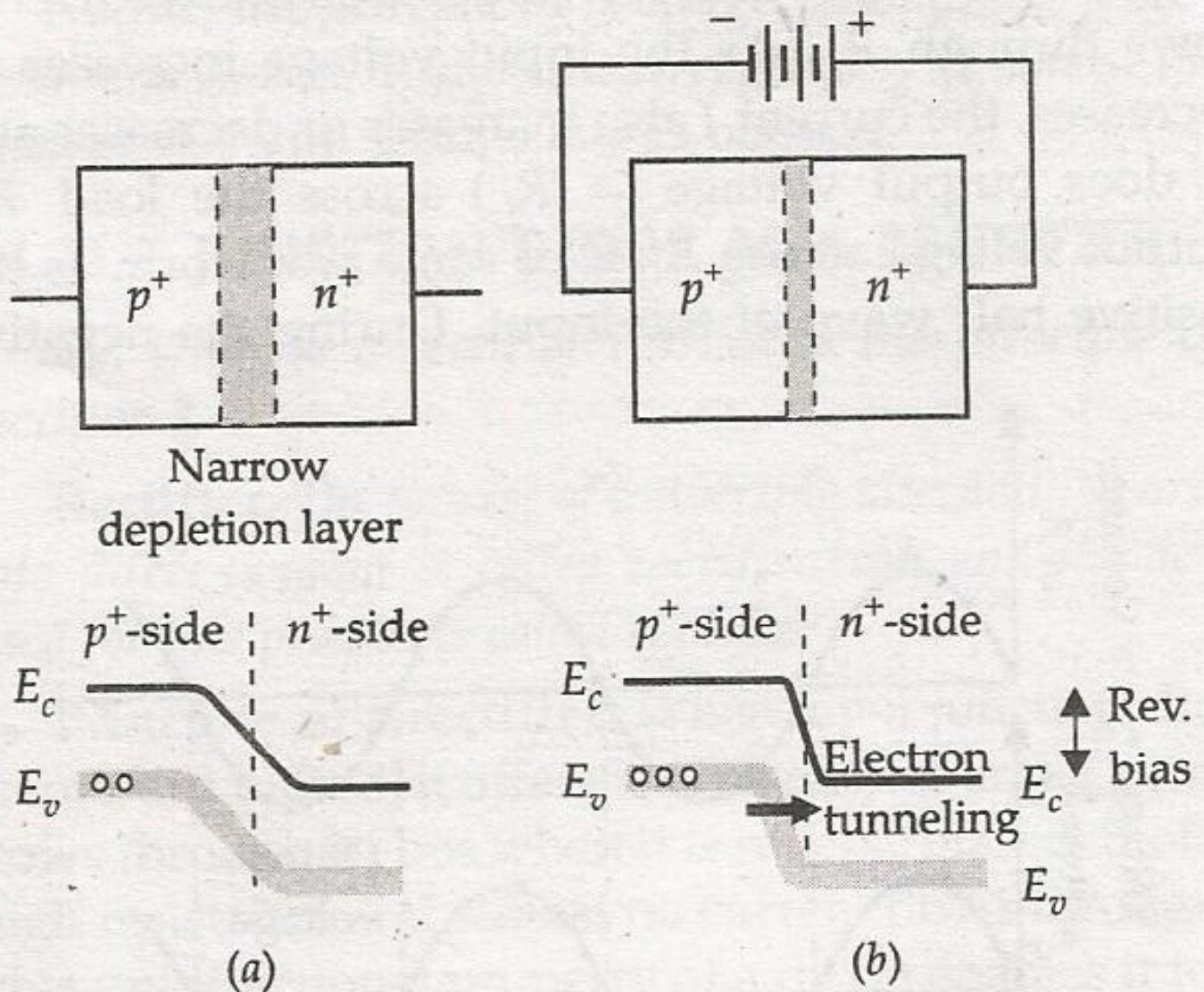
Fig. 14.28 (a) Unbiased $p^+ - n^+$ and (b) reverse biased $p^+ - n^+$ junctions of a Zener diode.

both p- and n-sides are heavily doped by acceptor and donor impurities respectively. Due to high dopant density, the width of the junction layer is small and the barrier field ($E = V / d$) is high.

When a large reverse bias is applied across such a diode, the depletion layer and the energy bands get modified, as shown in Fig. 14.28(b). As the depletion width is very small ($< 10^{-7}$ m), even a small voltage (say 4 V) will set up a high electric field of 4×10^7 Vm^{-1}. This high electric field strips off many electrons from valence band which tunnel to the n-side through the thin depletion layer. This method of emission of electrons beyond a certain reverse bias voltage V_Z is called *internal field emission*. It gives rise to a large reverse current or breakdown current, as shown in Fig. 14.30. *This break-down in a diode due to the band-to-band tun-neling is called* **Zener breakdown** *and such diode is called* **Zener diode.** Here the breakdown voltage is of the order of few volts.


Fig. 14.29 V-I charac-teristic of a Zener diode.
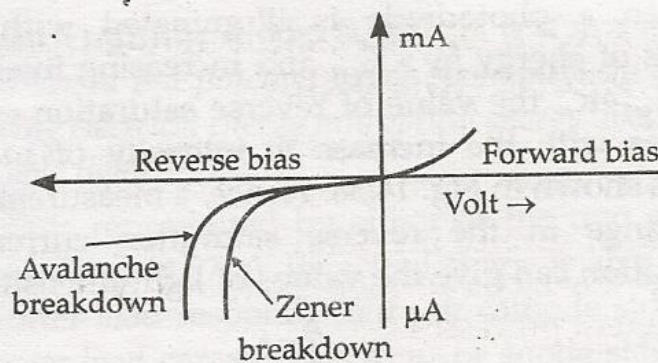
Fig. 14.30 V-I characteristic-curve for an avalanche diode.

2. Avalanche breakdown. This process occurs in diodes having low level of doping and hence wide depletion layer. When the reverse bias voltage is sufficiently high, the minority charge carriers get highly accelerated. Their kinetic energy becomes high enough and they *knock-off* electrons from the covalent bonds of the semiconductor. The newly generated electron-hole pairs also get accelerated and cause ionisation. Thus a chain of collisions is set up which gives rise to a very large number of charge carriers. This leads to a large reverse current, as shown in Fig. 14.30. This phenomenon is called *Avalanche breakdown* and the device is called *Avalanche diode.*

Zener diode. *A junction diode specially designed to operate only in the reverse breakdown region continuously (without getting damaged) is called a Zener diode. Zener diodes with different breakdown voltages can be obtained by changing the doping concentrations of p- and n-sides which, in turn, change the width of depletion layer and also the barrier field across the junction. The symbol of a Zener diode is shown in Fig. 14.31.*
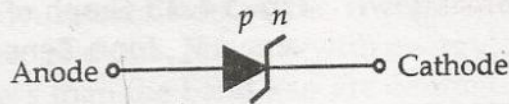
Fig. 14.31 Symbol for Zener diode.

Zener diode as a voltage regulator : Principle. *When a Zener diode is operated in the reverse breakdown region, the voltage across it remains practically constant (equal to the breakdown voltage V_Z) for a large change in the reverse current. The use of Zener diode as a d.c. voltage regulator is based on this fact.*

Working. Fig. 14.32 shows the circuit for using Zener diode as a voltage regulator. Here the Zener diode is connected in reverse bias to a source of fluctuating d.c. (e.g., the output from a rectifier) through a *dropping resistor R_S*. Thus the voltage gets divided between R and zener diode. The output is obtained across the load resistance R_L, connected in parallel with the zener diode.
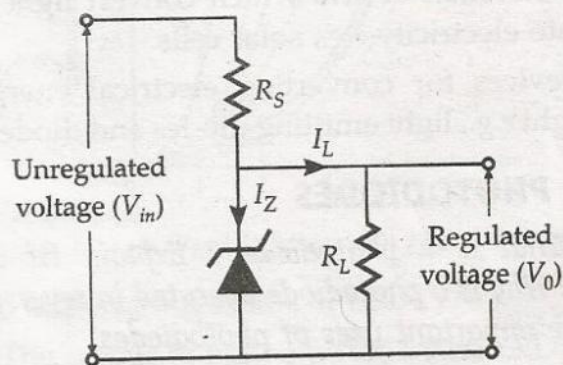

Fig. 14.32 Zener diode as a voltage regulator.

If the input voltage increases, the current through R_S and Zener diode also increases. This increases the voltage drop across R_S without any change in the voltage across the Zener diode. This is because in the breakdown region, Zener voltage remains constant even though the current through the Zener diode changes. Similarly, if the input voltage decreases, the voltage across R_S decreases without any change in the voltage across the Zener diode. Thus any increase/decrease of the input voltage results in, increase/decrease of the voltage drop across R_S without any change in voltage across Zener diode. Hence the Zener diode acts as a voltage regulator.

Fig. 14.33 shows the graph of output voltage V_0 versus input voltage V_{in} for a Zener diode. Clearly, the output voltage remains constant after the reverse breakdown voltage V_Z.
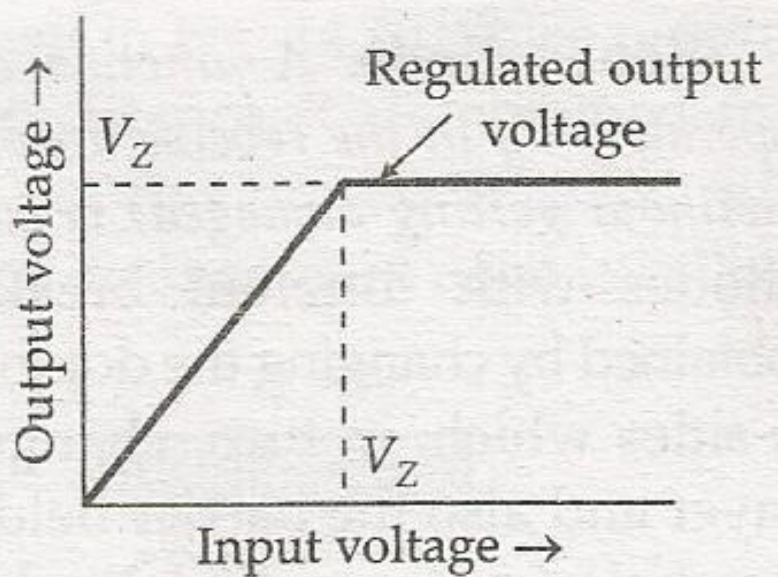

Fig. 14.33 Graph of V_0 versus V_{in} for a Zener diode.

14.22 ▼ JUNCTION DIODE AS A HALF-WAVE RECTIFIER

26. With the help of half a circuit diagram, explain the use of a junction diode as a half-wave rectifier. Draw the input and output waveforms.

Junction diode as a half-wave rectifier. A half-wave rectifier consists of a transformer, a junction diode D and a load resistance R_L. The primary coil of the transformer is connected to the a.c. mains and the secondary coil is connected in series with the junction diode D and load resistance R_L. We assume that the diode is ideal so that it offers infinite resistance during the reverse biasing.
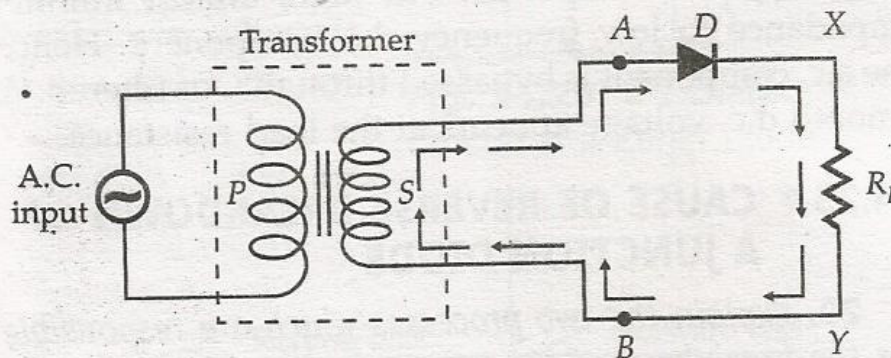
Fig. 14.22 Half-wave rectifier circuit.

Working. When a.c. is supplied to the primary, the secondary of the transformer supplies desired alternating voltage across A and B. During the positive half cycle of a.c., the end A is positive and the end B is negative. The diode D is forward biased and a current I flows through R_L. As the input voltage increases or decreases, the current I also increases or decreases and so does output voltage ($= IR_L$) across the load R_L. Output voltage across R_L is of same waveform as the positive half wave of the input. During the negative
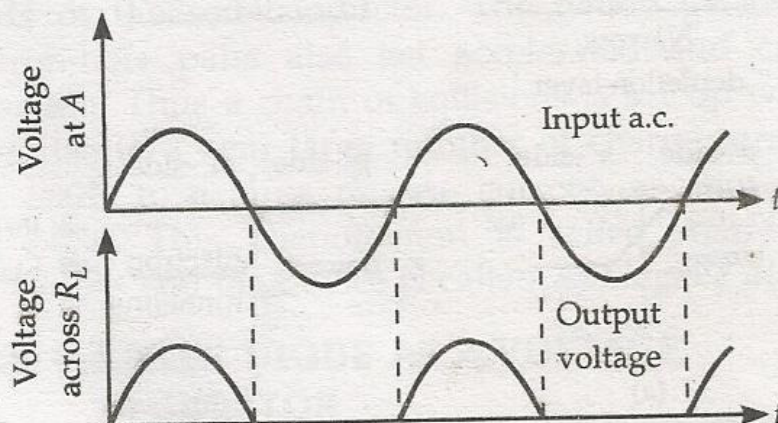
Fig. 14.23. Waveforms of input a.c. and output voltage obtained from a half-wave rectifier.

half cycle, the end A becomes negative and B positive. The diode is reverse biased and no current flows. No voltage appears across R_L. In the next positive half cycle, again we get output voltage. The output voltage is unidirectional but pulsating, as shown in Fig. 14.23. Since the voltage across the load appears only during the positive half cycle of the input *a.c.*, this process is called *half-wave rectification* and the arrangement used is called a *half-wave rectifier*.

14.23 ▼ JUNCTION DIODE AS A FULL WAVE RECTIFIER

27. *With the help of a circuit diagram, explain full wave rectification using junction diodes. Draw the waveforms of input and output voltages.*

Junction diode as a full wave rectifier. A full wave rectifier consists of a transformer, two junction diodes D_1 and D_2 and a load resistance R_L. The input a.c. signal is fed to the primary coil P of the transformer. The two ends A and B of the secondary S are connected to the p-ends of diodes D_1 and D_2. The secondary is tapped at its central point T which is connected to the n-ends of the two diodes through the load resistance R_L, as shown in Fig. 14.24.
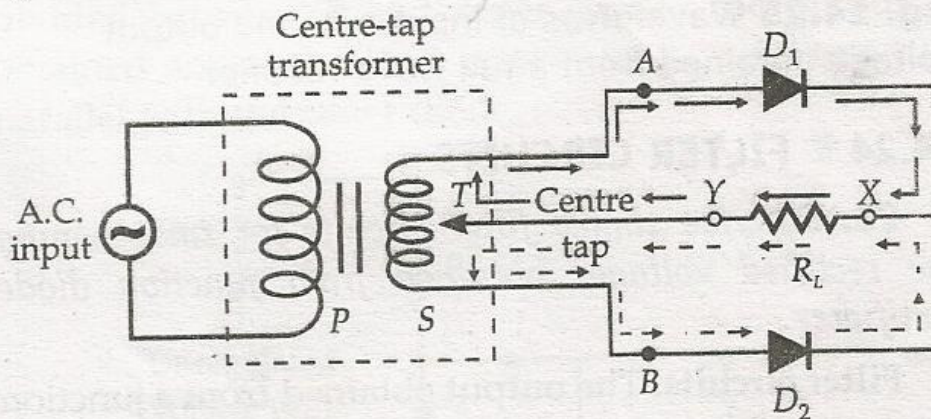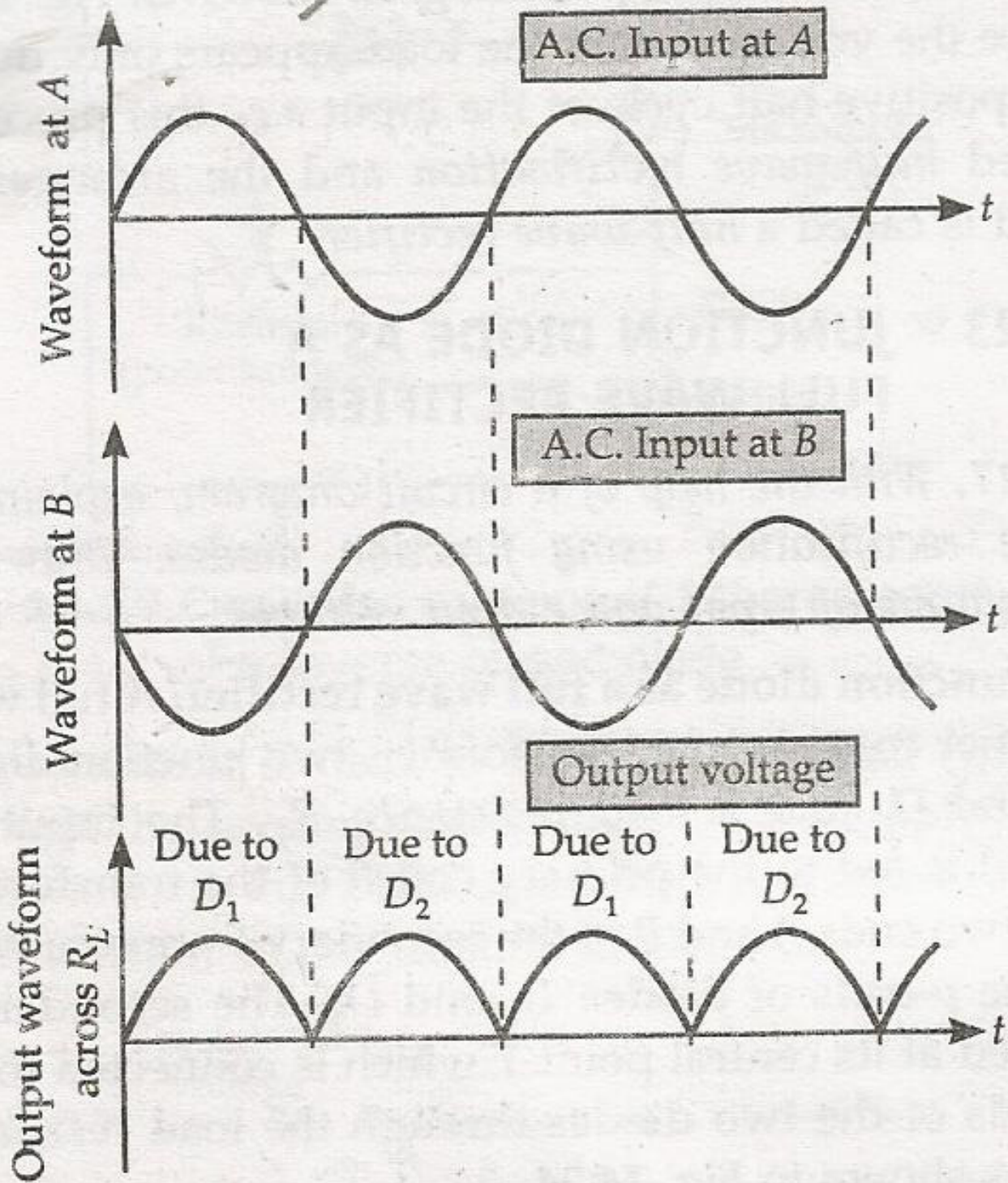

Fig. 14.24 Full wave rectifier circuit.

Working. At any instant, the voltages at the end A (input of D_1) and end B (input of D_2) of the secondary with respect to the centre tap T will be out of phase with each other. Suppose during the positive half cycle of a.c. input, the end A is positive and the end B is negative with respect to the centre tap T. Then the diode D_1 gets forward biased and conducts current along the path $AD_1 XYTA$, as indicated by the solid arrows. The diode D_2 is reverse biased and does not conduct. During the negative half cycle, the end A becomes negative and the end B becomes positive with respect to the centre tap T. The diode D_1 gets reverse biased and does not conduct. The diode D_2 conducts current along the path $BD_2 XYTB$, as indicated by broken arrows. As during both half cycles of input a.c. the current through load R_L flows in the same direction $(X \rightarrow Y)$, so we get a pulsating d.c.

voltage across R_L, as shown in Fig. 14.25. Since output voltage across the load resistance R_L is obtained for both half cycles of input a.c., this process is called *full wave rectification* and the arrangement used is called *full-wave rectifier.*

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Fig. 14.25 Waveforms of input a.c. and output voltage obtained from a full wave rectifier.

14.18 ▼ WORKING OF A p-n JUNCTION

**22.** *Explain the working of a junction diode when it is (i) forward biased and (ii) reverse biased.*

Working of a p-n junction. An external potential difference can be applied to a p-n junction in two ways :

1. Forward biasing. *If the positive terminal of a battery is connected to the p-side and the negative terminal to the n-side, then the p-n junction is said to be forward biased.*

As shown in Fig. 14.15(a), here the applied voltage V opposes the barrier voltage V_B. As a result of this

(i) the effective barrier potential decreases to $(V_B - V)$ and hence the energy barrier across the junction decreases, as shown in Fig. 14.15(b),

(ii) the majority charge carries *i.e.*, holes from p-side and electrons from n-side begin to flow towards the junction,

(iii) the diffusion of electrons and holes into the depletion layer decreases its width, and

(iv) the effective resistance across the p-n junction decreases.
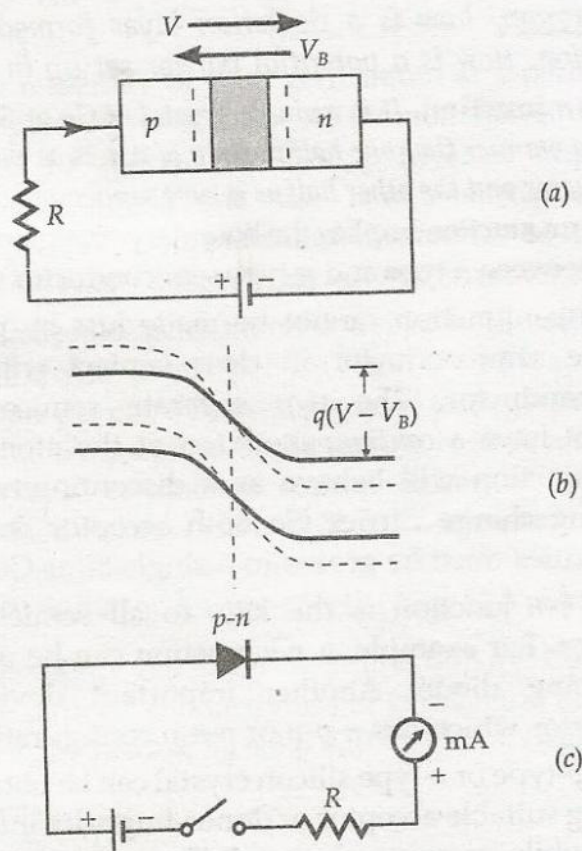
Fig. 14.15 (a) Reduced depletion layer, (b) Reduced energy barrier, (c) Symbolic representation, for a forward biased p-n junction.

When V exceeds V_B, the majority charge carriers start flowing easily across the junction and set up a large current ($\approx$ mA), called forward *current*, in the circuit. The current increases with the increase in applied voltage.

2. Reverse biasing. *If the positive terminal of a battery is connected to the n-side and negative terminal to the p-side, then the p-n junction is said to be reverse biased.*

As shown in Fig. 14.16 (a), the applied voltage V and the barrier potential V_B are in the same direction. As a result of this

(i) the barrier potential increases to $(V_B + V)$ and hence the energy barrier across the junction increases,
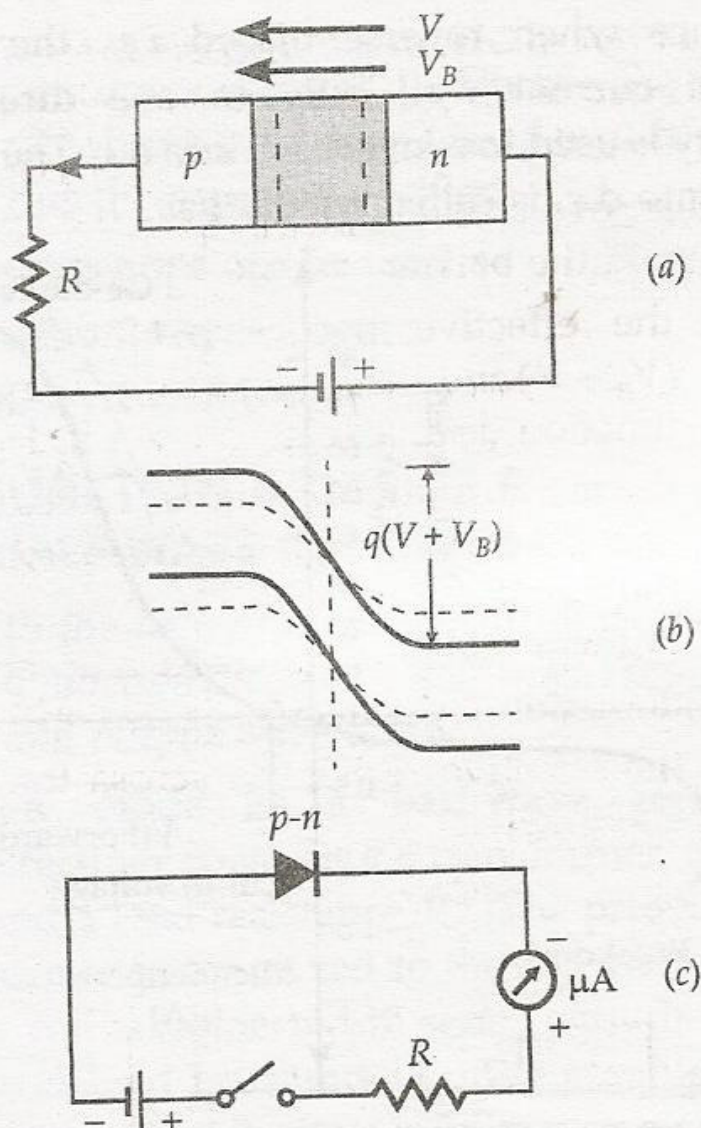
Fig. 14.16 (a) Increased depletion layer,
(b) Increased energy barrier, (c) Symbolic
representation for a reverse biased p-n junction.

(ii) the majority charge carriers move away from the junction, increasing the width of the depletion layer,

(iii) the resistance of the p-n junction becomes very large, and

(iv) no current flows across the junction due to majority charge carriers.

However, at room temperature there are always present some minority charge carriers like holes in n-region and electrons in p-region. The reverse biasing pushes them towards junction, setting a current, called *reverse or leakage current*, in the external circuit in the opposite direction. As the minority charge carriers are much less in number than the majority charge carriers, hence the reverse current is small ($\approx \mu A$).
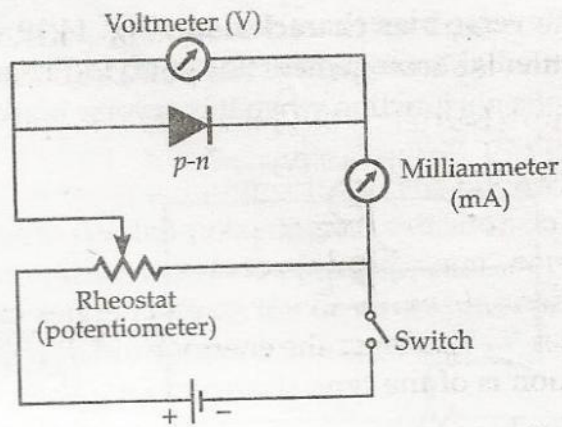
14.19 ▼ V-I CHARACTERISTICS OF A p-n JUNCTION DIODE

23. *With the help of suitable circuit diagrams, explain how will you sketch the characteristic curves of a junction diode. Sketch and explain these curves.*

V-I characteristics of a p-n junction diode. *A graph showing the variation of current flowing through a p-n junction with the voltage applied across it (both when it is forward and reverse biased) is called the voltage-current or V-I characteristic of a p-n junction*

**1. Forward bias characteristic.** Fig. 14.17 shows the experimental arrangement for studying the characteristic curve of a p-n junction when it is *forward*

Fig. 14.17 Circuit for studying V-I characteristic of a forward biased diode.

biased. A battery is connected across the p-n junction diode through a potentiometer (or rheostat) so that the voltage applied to the diode can be changed. The milliammeter measures the current through the diode and the voltmeter measures the voltage across the diode. For different values of voltages, the value of current is noted. A graph is plotted between V and I, as shown in Fig. 14.18. This voltage-current graph is called *forward characteristic*.
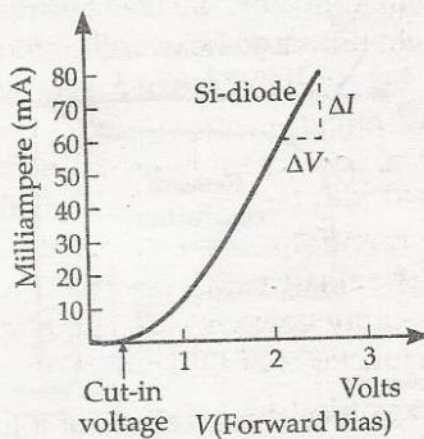

Fig. 14.18 Forward characteristic of a junction diode.

Important features of the graph. (*i*) The V-I graph is not a straight line *i.e.*, a junction diode does not obey *Ohm's law*.

(*ii*) Initially, the current increases very slowly almost negligibly, till the voltage across the diode crosses a certain value, called the **threshold-voltage** or **cut-in voltage**. The value of the cut-in voltage is about 0.2 V for a Ge diode and 0.7 V for a Si diode. Before this characteristic voltage, the depletion-layer plays a dominant role in controlling the motion of charge carriers.

(*iii*) After the cut-in voltage, the diode current increases rapidly (exponentially), even for a very small increase in the diode bias voltage. Here the majority charge carriers feel negligible resistance at the junction *i.e.*, the resistance across the junction is quite low.

2. Reverse bias characteristic. Fig. 14.19 shows the experimental arrangement for studying characteristic curve of a p-n junction when it is reverse biased. Here a
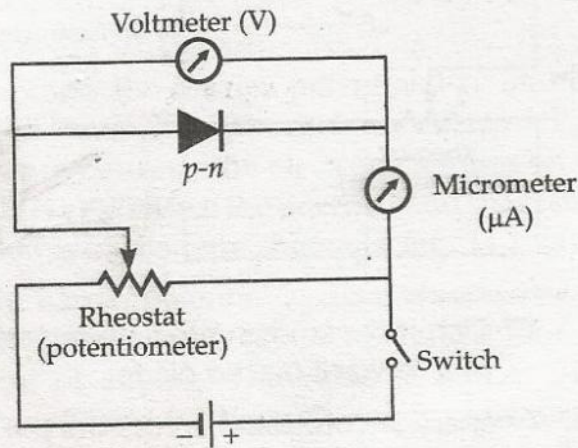
Fig. 14.19 Circuit for studying V-I characteristic of a reverse biased diode.

microammeter is used to measure the small currents through the reverse biased diode. A V-I graph of the type shown in Fig. 14.20 is obtained. It is called *reverse characteristic* of the junction diode.
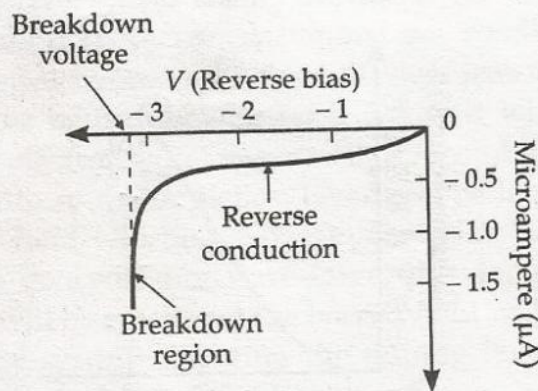
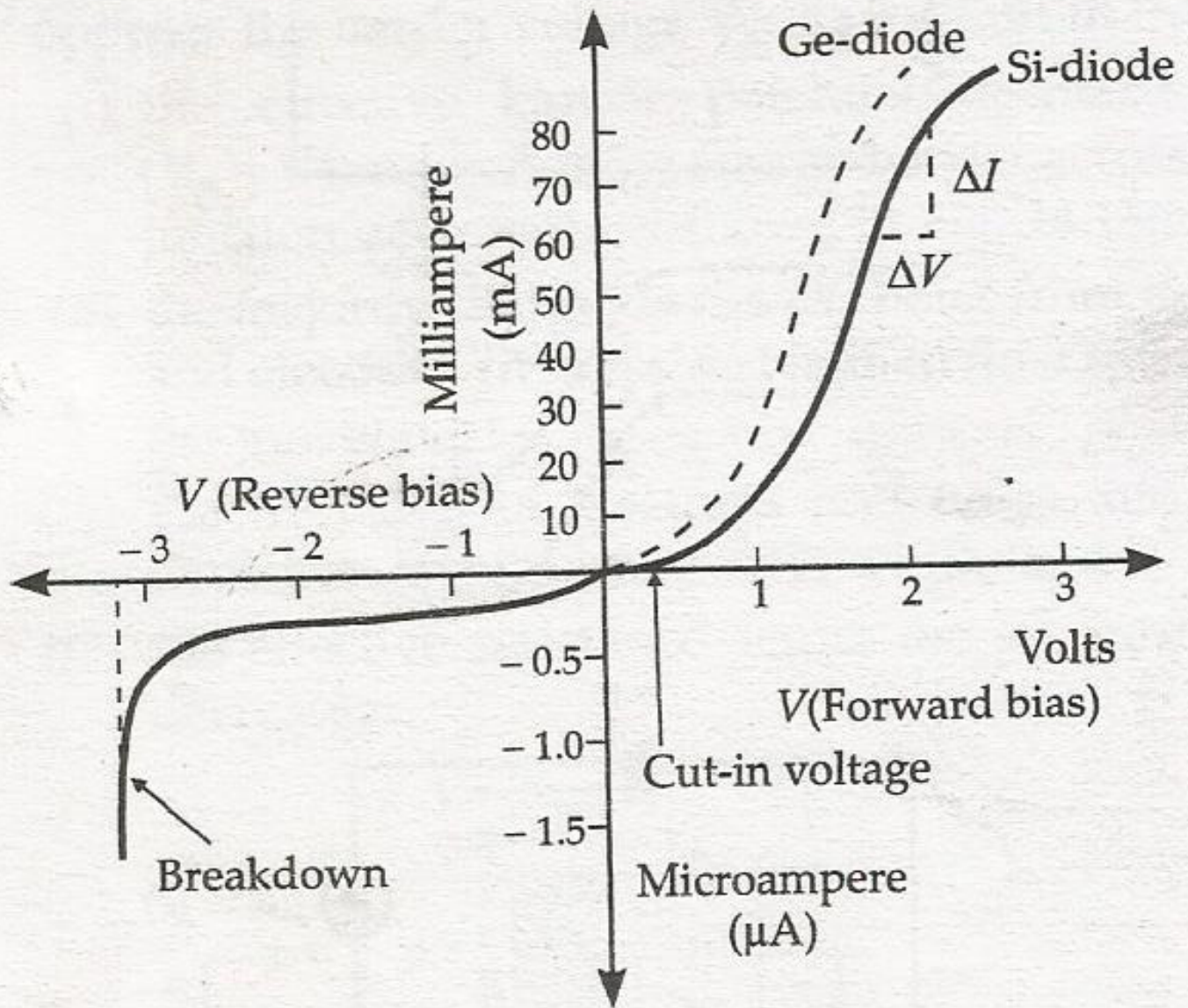**Fig. 14.20** Reverse characteristic of a junction diode.

Important features of the graph. (*i*) When the diode is reverse biased, the reverse bias voltage produces a very small current, about a few microamperes which almost remains constant with bias. This small current is called *reverse saturation current*. It is due to the drift of minority charge carriers (a few holes in *n*-region and a few electrons in *p*-region) across the junction.

(*ii*) When the reverse voltage across the *p-n* junction reaches a sufficiently high value, the reverse current suddenly increases to a large value. This voltage at which breakdown of the junction diode occurs is called *Zener breakdown voltage* or *peak-inverse voltage* of the diode. It ranges from as low as 1 to 2 V to several hundred volts, depending on the dopant density and the depletion layer.

Fig. 14.21 shows the complete V-I characteristic of a *p-n* junction. Obviously, it is a *unidirectional current* characteristic. A junction diode offers a very small resistance when forward biased and has a very large

resistance when reverse biased *i.e.*, the diode can conduct current well only in one direction. This property is used to convert a.c. into d.c. The conversion of a.c. into d.c. is called *rectification*.

Fig. 14.21 Complete *V-I* characteristic of a junction diode.

21. *What is a p-n junction ? Explain with the help of a diagram, how is a depletion layer formed near its junction. How is a potential barrier set up in it ?*

p-n junction. *It is a single crystal of Ge or Si doped in such a manner that one half portion of it acts as p-type semiconductor and the other half as n-type semiconductor. Here, the term junction implies the boundary or region of transition between n-type and p-type semiconductor materials.*

A *p-n* junction cannot be made just by placing a *p*-type semiconductor in close contact with *n*-type semiconductor. The two separate semiconductors cannot have a *continuous contact* at the atomic level. The junction will behave as a discontinuity for the flowing charge carries. So both acceptor and donor impurities must be grown in a single Si or Ge crystal.

A *p-n* junction is the key, to all semiconductor devices. For example, a *p-n* junction can be used as a rectifying diode. Another important device is a transistor which has *n-p-n* or *p-n-p* configuration.

A *p*-type or *n*-type silicon crystal can be obtained by adding suitable acceptor or donor-impurity into silicon melt while growing a crystal. These crystals are cut into thin slices called *wafers*. Semiconductor devices are usually made on these wafers.

Unbiased *p-n* junction : Depletion region and potential barrier in a *p-n* junction. As soon as a *p-n* junction is formed, the majority charge carriers begin to diffuse from the regions of higher concentration to the regions of lower concentrations. Thus the electrons from the *n*-region diffuse into the *p*-region and where they combine with the holes and get neutralised. Similarly, the holes from the *p*-region diffuse into the *n*-region where they combine with the electrons and get neutralised. This process is called *electron-hole recombination*.

The *p*-region near the junction is left with immobile – ve ions and *n*-region near the junction is left with + ve ions, as shown in Fig. 14.13(*a*). *The small region in the vicinity of the junction which is depleted of free charge carriers and has only immobile ions is called the **depletion layer**.*
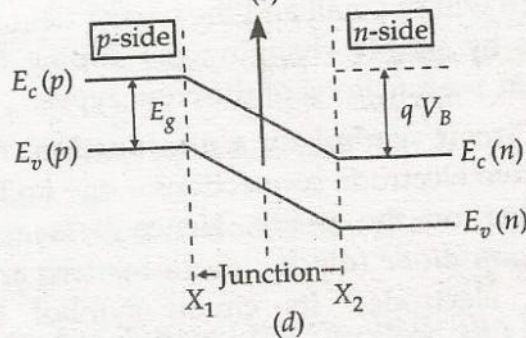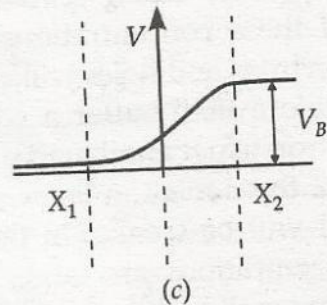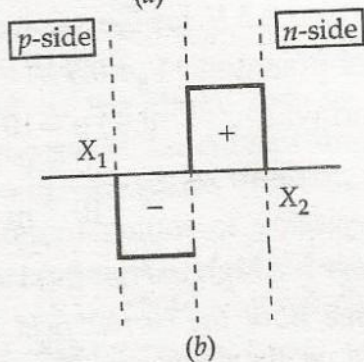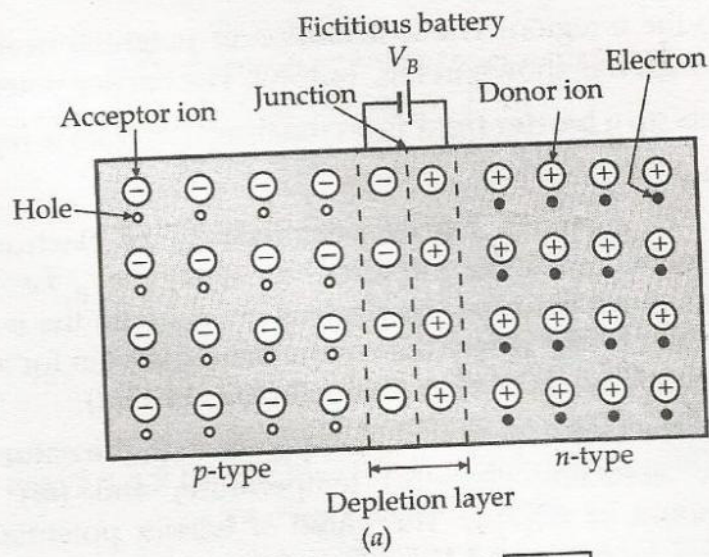
Fig. 14.13. Formation of *p-n* junction : (*a*) depletion layer consisting of immobile –ve and +ve ions (*b*) charge accumulation (*c*) barrier potential and (*d*) energy band diagram.

The distribution of charge near the junction is shown in Fig. 14.13(*b*).

The accumulation of negative charges in the *p*-region and positive charges in the *n*-region sets up a potential difference across the junction. This acts as a barrier and is called barrier potential V_B which opposes the further diffusion of electrons and holes across the junction. It appears as if a sort of fictitious battery has been set up across the junction with the – ve terminal connected to the *p*-region and + ve terminal connected

to the n-region. The distribution of potential near the junction is shown in Fig. 14.13(c). The barrier potential sets up a **barrier field** $\vec{E}_B$ in the direction from n-region to p-region.

To cross the barrier potential V_B, an electron of n-region must be imparted an energy eV_B i.e., the difference between the electron energies on the n-and p-sides is eV_B. Hence the energy band diagram for a p-n junction is of the type shown in Fig. 14.13(d).

The barrier potential V_B depends on (i) the nature of the semiconductor, (ii) temperature, and (iii) the amount of doping. The value of barrier potential is 0.7 V for Si and 0.3 V for Ge semiconductors.

If barrier potential, $V_B \simeq 0.5$ V

depletion width, $d \simeq 1\mu = 10^{-6}$ m

then, electric field, $E_B \simeq \dfrac{0.5\text{ V}}{10^{-6}\text{ m}} = 5 \times 10^5$ Vm^{-1}

Thus there is a high barrier field across the junction.

Let us see how *the barrier field and depletion layer width depend on the doping concentrations in the n- and p-regions.* If these concentrations are small, then the diffusing electrons and holes will cover reasonably large distances before they suffer a collision with another hole or electron to get annihated or recombined. Hence the width of the depletion layer will be large and the barrier field will be weak. On the other hand, if the doping concentrations are large, the depletion layer width will be small and the barrier field will be strong. Thus by simply changing the doping levels, we can obtain p-n junctions of different types.

Circuit symbol for a p-n junction. A p-n junction has two electrode connections – one on the p-side and another on the n-side. Hence it is also known as *junction diode* (diode : di-means two and ode comes from electrode). Its circuit symbol is shown in Fig. 14.14. The direction of the arrow is from p-region to n-region. The arrow indicates the direction in which the conventional current can flow easily (when the diode is forward biased). The p-side is known as the *anode* and the n-side is known as the *cathode*.
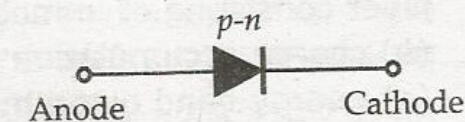

Fig. 14.14 Symbol for a p-n junction diode.

14.9 ▼ ENERGY BANDS OF INTRINSIC AND EXTRINSIC SEMICONDUCTORS

13. *Sketch and explain the energy band diagrams of intrinsic and extrinsic semiconductors.*

Energy band diagram of intrinsic semiconductors. At $T = 0$ K, the valence band of a semiconductor is completely filled with electrons while the conduction band is empty, as shown in Fig. 14.11[a(i)]. Hence an intrinsic semiconductor behaves like an insulator at $T = 0$ K. At higher temperatures $(T > 0$ K), some electrons of the valence band gain sufficient thermal

(*i*) at $T = 0$ K
(behaves like insulator)

(*ii*) at $T > 0$ K
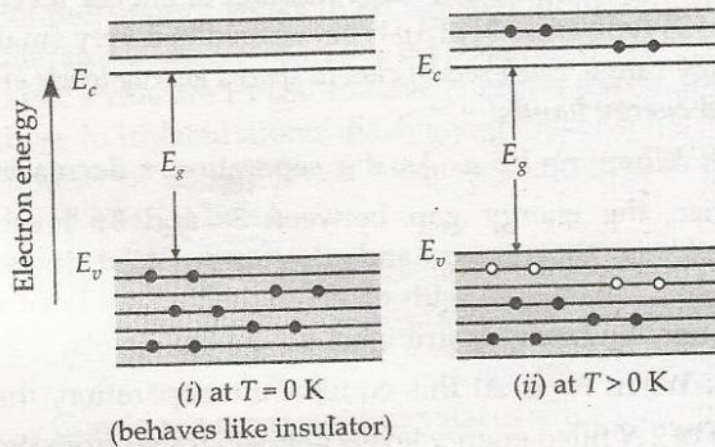
Fig. 14.11 (*a*) Energy band diagrams of intrinsic semiconductor

energy and jump to the conduction band, creating an equal number of holes in the valence band. These thermally excited electrons occupy the lowest possible energy levels in the conduction band. Therefore, the energy band diagram of an intrinsic semiconductor at $T > 0$ K is of the type shown in Fig. 14.11[a(ii)]. Clearly, the number of electrons in conduction band is equal to the number of holes in valence band.

Energy band diagram of n-type semiconductor. In n-type semiconductors, the extra (fifth) electron is very weakly attracted by the donor impurity. A very small energy (≈ 0.01 eV) is required to free this electron from the donor impurity. When freed, this electron will occupy the lowest possible energy level in the conduction band *i.e.*, the energy of the donor electron is slightly less than E_c. Thus *the donor energy level E_D lies just below the bottom of the conduction band* as shown in Fig. 14.11(b). At room temperature this small energy gap is easily covered by the thermally excited electrons. The conduction band has more
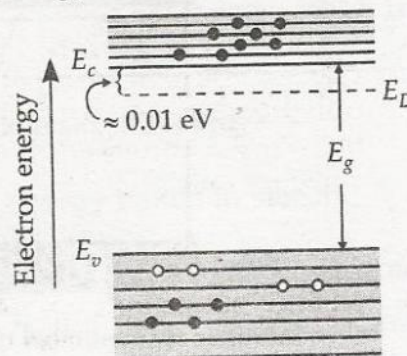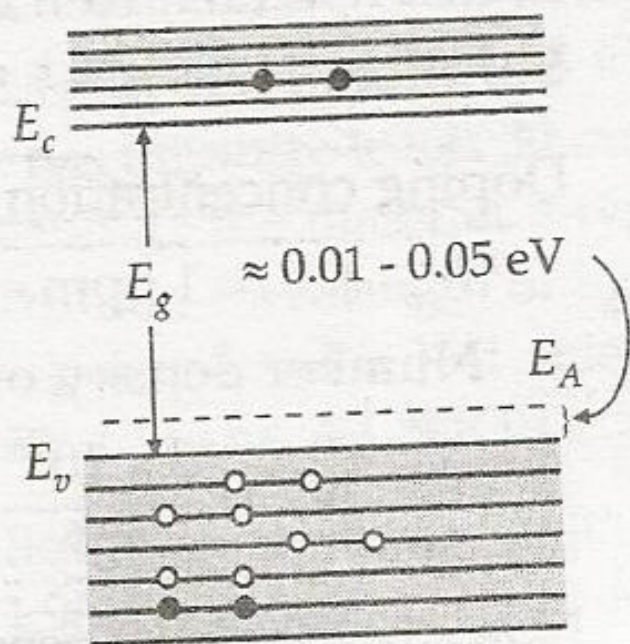

Fig. 14.11 (*b*) Energy band diagram of n-type semiconductor at $T > 0$ K

electrons (than holes in valence band) as they have 1₄
been contributed both by thermal excitation and donor
impurities.

Energy band diagram of p-type semiconductors. cₒ
In p-type semiconductors, each acceptor impurity
creates a hole which can be easily filled by an electron
of Si-Si covalent bond i.e., a very small energy
($\approx 0.01 - 0.05$ eV) is required by an electron of the
valence band to move into this hole. Hence the
acceptor energy level E_A lies slightly above the top of
the valence band, as
shown in Fig. 14.11(c). At
room temperature, many
electrons of the valence
band get excited to these
acceptor energy levels,
leaving behind equal
number of holes in the
valence band. These holes
can conduct current. Thus
the valence band has more
holes than electrons in the
conduction band.

E_c

E_g $\approx 0.01 - 0.05$ eV

E_A

E_v

Fig. 14.11 (c) Energy
band diagram of p-type
semiconductor at $T > 0$ K.

BETWEEN INTRINSIC