MNEMOSENE
computation-in-memory architecture based on resistive devices

Newsletter No. 2
Jan 2019 - Jun 2019
www.mnemosene.eu

MNEMOSENE at a glance

MNEMOSENE is an ambitious research and innovation action addressing the theme "*Development of new approaches to scale functional performance of information processing and storage substantially beyond the state-of-the-art technologies with a focus on ultra-low power and high performance*" of the EU's Horizon 2020 ICT research and innovation programme. The project will last 3 years and has been funded with a total of 4M €. Coordinated by Said Hamdioui at Delft Technical University (NL), the MNEMOSENE Consortium include Eindhoven University of Technology and IMEC (NL), ETH Zurich and IBM Research – Zurich (CH), Arm (UK), RWTH Aachen University (DE), INRIA (FR) and Intelligentsia Consultants (LU).

In order to meet the requirements of future electronic applications, MNEMOSENE will focus on the development, design and demonstration of a Computation-In-Memory (CIM) architecture based on extending arrays of non-volatile resistive switching devices (memristors) with logic functionality inside or around the cell array.

MNEMOSENE officially started in January 2018 and has now successfully concluded its first 18 months of activities. Important results have been achieved and disseminated through peer-review publications and participation to conferences and seminars.

News

25-29.03.2018 - MNEMOSENE booth at DATE 2019. Several members of the MNEMOSENE consortium took part in DATE (Design, Automation and Test in Europe) conference in Florence (IT) on 25-29 March 2019, presenting results obtained during the first year of the project. MNEMOSENE was also present with a dedicated booth, where team members had the chance to illustrate project's objectives and initial results.

MNEMOSENE booth at DATE (Design, Automation and Test in Europe) Conference 2019 in Florence (IT)

Project Meetings

Project meetings in 2019 have been organised according to the work plan and included monthly conference calls at both project and WP levels:

- [31.01.19] M12 Project Meeting (Zürich, CH)

Upcoming meetings

- [11.07.19] M18 Project meeting (Dresden, DE), during MEMRISYS Conference.

European Commission

The MNEMOSENE project has received funding from the European Union's Horizon 2020 Research and Innovation Programme under grant agreement No 780215.

Publications

After 18 months from the project start, research supported by MNEMOSENE has already resulted in several publications in peer-reviewed journals and conference proceedings. All publications have been made open access through self-archiving in different repository. In the period between January and June 2019, the following papers have been published in peer review journals and conference proceedings:

[1] A. Burrello, L. Cavigelli, K. Schindler, L. Benini, A. Rahimi, ''*Laelaps: An Energy-Efficient Seizure Detection Algorithm from Long-term Human iEEG Recordings without False Alarms*'' in proceedings of the 2019 ACM/IEEE Design, Automation, and Test in Europe Conference (DATE), Florence, Italy, March 25-29, 2019. DOI: 10.3929/ethz-b-000307983

[2] J. Yu, H. A. Du Nguyen, M. A. Lebdeh, M. Taouil, S. Hamdioui, "*Time-division Multiplexing Automata Processor*" in proceedings of the 2019 ACM/IEEE Design, Automation, and Test in Europe Conference (DATE), Florence, Italy, March 25-29, 2019. DOI: 10.5281/zenodo.2533075

[3] S. Hamdioui, H. A. Du Nguyen, M. Taouil, A. Sebastian, M. Le Gallo, S. Pande, S. Schaafsma, F. Catthoor, S. Das, F. Garcia Redondo, G. Karunaratne, A. Rahimi, L. Benini. "*Applications of Computation-In-Memory Architectures based on Memristive Devices*" in proceedings of the 2019 ACM/IEEE Design, Automation, and Test in Europe Conference (DATE), Florence, Italy, March 25-29, 2019. DOI: 10.5281/zenodo.2533098

[4] M. Schmuck, L. Benini, A. Rahimi, "*Hardware Optimizations of Dense Binary Hyperdimensional Computing: Rematerialization of Hypervectors, Binarized Bundling, and Combinational Associative Memory*", in ACM Journal on Emerging Technologies in Computing, accepted for publication. DOI: 10.3929/ethz-b-000338354

[5] S. Benatti, F. Montagna, V. Kartsch, A. Rahimi, D. Rossi, L. Benini, "*Online Learning and Classification of EMG-Based Gestures on a Parallel Ultra-Low Power Platform using Hyperdimensional Computing*", in IEEE Transactions on Biomedical Circuits and Systems (TBioCAS), accepted for publication (2019). DOI: 10.3929/ethz-b-000339838

[6] K. Vadivel, P. Jääskeläinen, R. Jordans, H. Kultala, S. Stuijk, H. Corporaal, "*Towards Efficient Code Generation for Coarse-Grained Architectures*", in proceedings of the 22nd International Workshop on Software and Compilers for Embedded Systems, Sankt Goar (DE), May 27-28, 2019. DOI: 10.1145/3323439.3323990

[7] A. BanaGozar, S. Wong, M.A. Lebdeh, K. Vadivel, J. Yu, S. Hamdioui, S. Stuijk, H. Corporaal, "*CIM-SIM: Computation In Memory SIMulator*", in proceedings of the 22nd International Workshop on Software and Compilers for Embedded Systems, Sankt Goar (DE), May 27-28, 2019. DOI: 10.1145/3323439.3323989

[8] A. Siemon, S. Ferch, A. Heittmann, R. Waser, D. J. Wouters, S. Menzel, *"Analyses of Neuromorphic Networks using Memristive Devices with Non-continuous Resistance Levels"* , in APL Materials (submitted)

[9] F. Cüppers, S. Menzel, C. Bengel, A. Hardtdegen, M. von Witzleben, U. Böttger, R. Waser, S. Hoffmann-Eifert, *"Exploiting the switching dynamics of HfO2/TiOx-based ReRAM devices for reliable analogue memristive behaviour",* in APL Materials (submitted)

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Dissemination Events

The core of the dissemination and communication activities for MNEMOSENE started on M13 (Jan 19) and the Project Coordinator and other Consortium members are now actively promoting MNEMOSENE during international conferences and workshops. A full list of events where MNEMOSENE was promoted between January and June 2019 is reported below.

- [25-29.03.19] Presentation: "*Laelaps: An Energy-Efficient Seizure Detection Algorithm from Long-term Human iEEG Recordings without False Alarms*", A. Burrello, DATE (Design, automation and test in Europe) Conference 2019 (Florence, IT)
- [25-29.03.19] Presentation: "*Time-division Multiplexing Automata Processor*", J. Yu, DATE (Design, automation and test in Europe) Conference 2019 (Florence, IT)
- [25-29.03.19] Presentation: *"Applications of Computation-In-Memory Architectures based on Memristive Devices"*, S. Hamdioui, DATE (Design, automation and test in Europe) Conference 2019 (Florence, IT)
- [25-29.03.19] Invited Talk: "*Computation-in-Memory Based on Memristive Devices: What is all about and what is still missing? "*, S. Hamdioui, DATE (Design, automation and test in Europe) Conference 2019 (Florence, IT)
- [26-29.05.19] Presentation: *"Memristive Device Modeling and Circuit Design Exploration for Computation-in-Memory"*, A. Siemon, ISCAS (IEEE International Symposium on Circuits and Systems) Conference 2019 (Sapporo, JP)
- [26-29.05.19] Presentation: *"Memristive Device Based Circuits for Computation-in-Memory Architectures"*, M.A. Lebdeh, ISCAS (IEEE International Symposium on Circuits and Systems) Conference 2019 (Sapporo, JP)
- [26-29.05.19] Full-day tutorial: *"Memristive Devices: From device physics to memristive circuits"*, S. Menzel, ISCAS (IEEE International Symposium on Circuits and Systems) Conference 2019 (Sapporo, JP)
- [27-28.05.19] Presentation: *"Towards Efficient Code Generation for Coarse-Grained Architectures"*, K. Vadivel, 22nd International Workshop on Software and Compilers for Embedded Systems (Sankt Goar, DE)
- [27-28.05.19] Presentation: *"CIM-SIM: Computation In Memory SIMulator"*, A. BanaGozar, 22nd International Workshop on Software and Compilers for Embedded Systems (Sankt Goar, DE)

Upcoming Events:

- [08-11.07.19] Presentation: *"Simulation of Abrupt SET and Gradual RESET Behavior in Variable HfO2/TiOx ReRAM Cell",* C. Bengel, International Conference on Memristive Materials, Devices & Systems (MEMRISYS) 2019 (Dresden, DE)

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