PLL FM Transmitter

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This is a circuit that offers a challenge to electronics enthusiasts and hobbyists—an FM transmitter that uses readily available components and covers the FM broadcast band in 100kHz steps. The frequency drift is controlled by phase-locked-loop (PLL) method, making transmission frequency rock-solid all the time, just like commercial stations. Using DIP switches, simply punch in the frequency on which you wish to broadcast, and you are on the air.

Circuit and working

The circuit comprises two units. Unit 1 is the RF section of the transmitter, shown in Fig. 1, which transmits the FM signal. Unit 2 is the PLL control section, shown in Fig. 2, which helps in locking the transmission frequency. The circuit uses phase-lock loop that provides drift-free transmission frequency.

The RF section is built around transistors T1-T4, with T1 (2N2222) in Colpitts oscillator configuration. The frequency of the oscillator is determined by coil L1 and capacitors C1, C2, C3 and C4. Modulating signal, which is in audio range, is fed through Jack1. D1 is a varactor diode, working in reverse-bias mode. Since this is an FM transmitter, the deviation in the frequency of the oscillator is based on the amount of reverse-bias generated by the audio signal. Transistor T2 (2N2222) acts as a buffer that isolates the oscillator from the rest of the amplifier chain.

Frequency-modulated signal is coupled to driver transistor T3 (BF199) via capacitor C5. R7 is a current-limiting resistor. Transistor T3 is wired as a Class A amplifier and drives transistor T4 (2N3866A) via broadband impedance matching transformer L2. Power amplifier operates in Class B mode. Coil L4 and trimmer capacitor VC1 match transistor T4's collector to the antenna.

The PLL control section is built around 64/256 prescaler SAB6456A (IC1), programmable divide-by-N counter CD4059(IC3), phase locked-loop comparator CD4046 (IC4), 14-stage ripple carry binary counter/oscillator

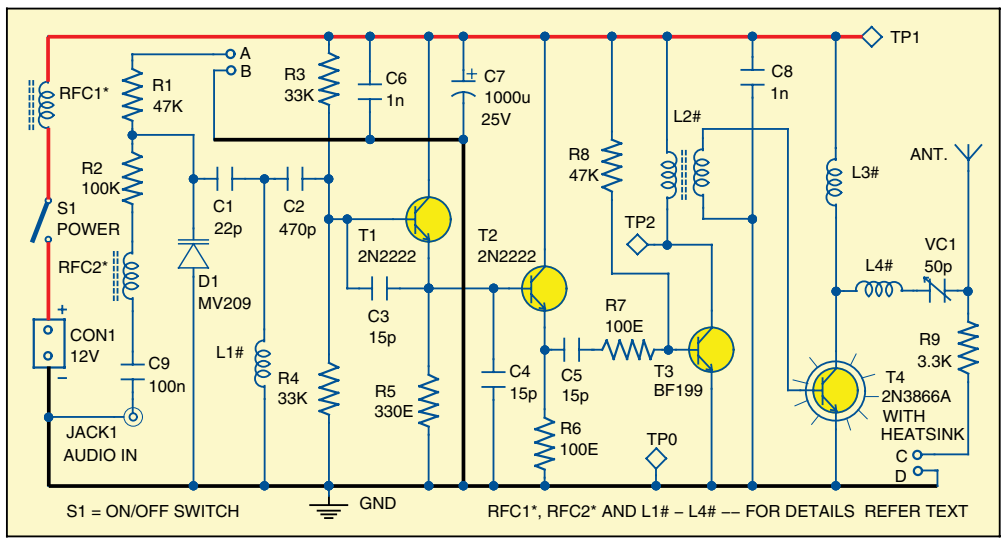

Fig. 1: RF section of the transmitter (Unit 1)

PARTS LIST

Semiconductors:

IC1	- SAB6456A 64/256 prescaler
IC2	- 7805 voltage regulator
IC3	- CD4059 programmable divide-by-N counter
IC4	- CD4046 phase-locked-loop (PLL) comparator
IC5	- CD4060 ripple carry binary counter/oscillator
IC6	- TL071 operational amplifier
T1, T2, T6	- 2N2222 npn transistor
T3, T5	- BF199 npn transistor
T4	- 2N3866A npn transistor
D1	- MV209 varactor diode
LED1	- 5mm LED

Resistors (all 1/4-watt, ±5% carbon):

R1, R8, R19-R31	- 47-kilo-ohm
R2, R15	- 100-kilo-ohm
R3, R4	- 33-kilo-ohm
R5	- 330-ohm
R6, R7	- 100-ohm
R9	- 3.3-kilo-ohm
R10	- 18-kilo-ohm
R11, R12, R16	- 10-kilo-ohm
R13	- 220-ohm
R14	- 2.2-kilo-ohm
R17	- 4.7-kilo-ohm
R18	- 1-mega-ohm
VR1	- 100-kilo-ohm preset

Capacitors:

C1, C16, C17	- 22pF, ceramic disk
C2	- 470pF ceramic disk
C3-C5	- 15pF ceramic disk
C6, C8	- 1nF ceramic disk
C7, C21	- 1000µF, 25V electrolytic
C9, C14, C18-C20, C22, C24	- 100nF ceramic disk
C10, C15	- 10µF, 25V electrolytic
C11	- 200nF ceramic disk
C12	- 400nF ceramic disk
C13	- 220µF, 25V electrolytic
VC1	- 50pF trimmer capacitor

Miscellaneous:

RFC1	- 50T, 28SWG balun core
RFC2	- 25T, 28SWG balun core
L1	- 4T, 4mm dia 26SWG
L2	- Broadband transformer 6T primary 26SWG, 1T secondary, 20SWG
L3	- 13T, 8mm dia 26SWG air core
L4	- 6T, 8mm dia 26 SWG air core
CON-CON2	- 2-pin terminal connector
$X_{TAL}1$	- 6.4MHz crystal
DIP1-DIP4	- DIP switch
S1, S2	- On/off switch
	- Audio input jack
	- Co-axial cable
	- Heat sink for transistor T4
	- Wire antenna

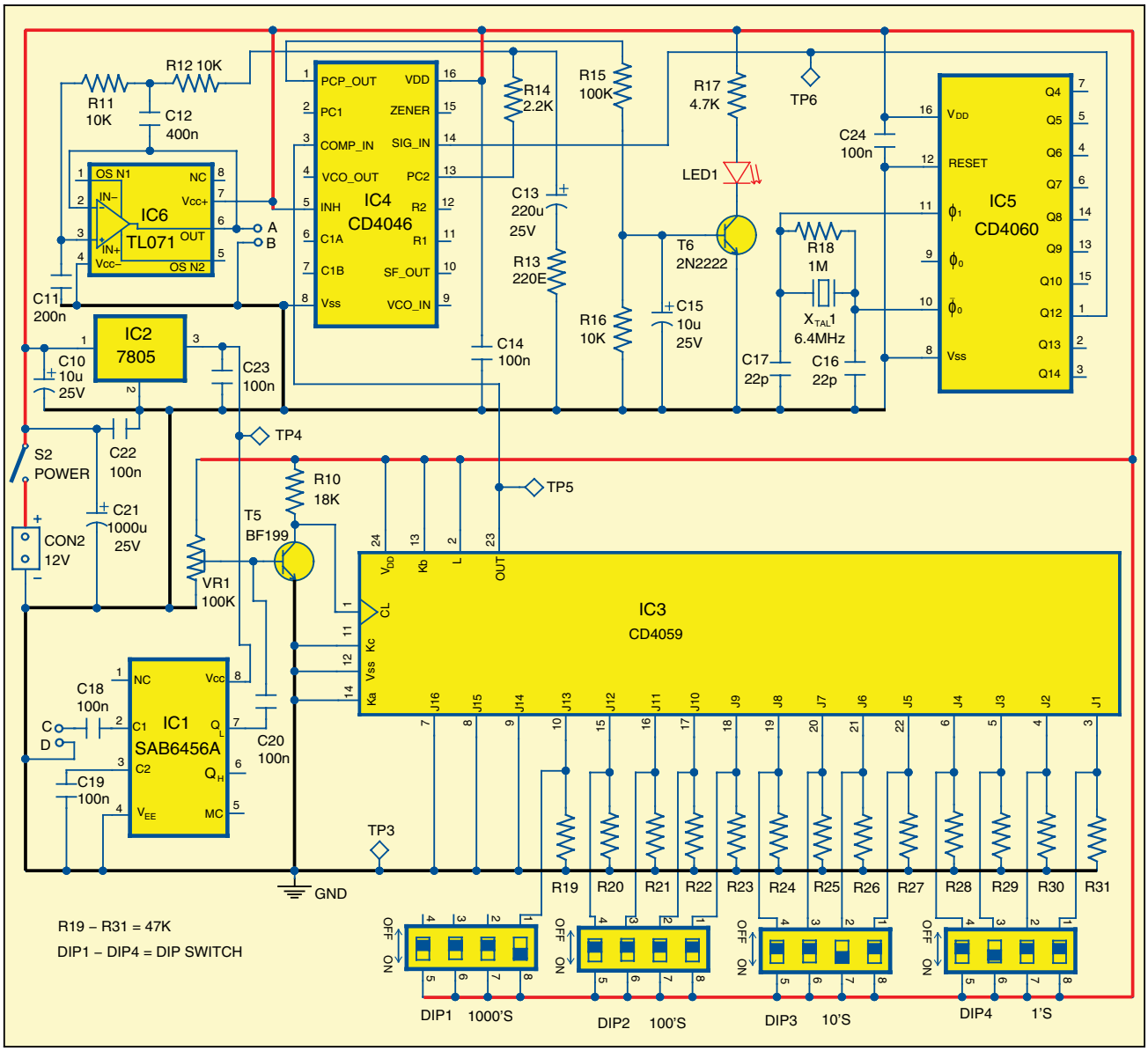

Fig. 2: PLL control section (Unit 2)

CD4060 (IC5) and operational amplifier TL071 (IC6).

This section uses voltage regulator 7805 (IC2) to provide regulated power supply of 5V for the working of IC1. IC5 generates 1.5625kHz reference frequency for the PLL at pin 1, which is fed to frequency comparator (IC4) at pin 14.

A low-level output is taken from the antenna via limiting resistor R9 (shown in Fig. 1), which is coupled to pin 2 of IC1 via capacitor C18. Pin 5 of IC1, the mode pin, is left open to select divide-by-64 mode. Output frequency of the transmitter is divided by 64. Transistor T5 converts the output of IC1 to 12V CMOS levels. The signal is further divided in programmable divide-by-N counter CD4059 (IC3). Output of CD4059 (pin 23) is connected to the frequency comparator pin 3 of IC4. The PLL comparator (IC4) compares the phase relationship between the reference signal on pin 14 with the input frequency on pin 3.

Depending upon the variance (phase relationship) up or down, a correction voltage is generated on pin 13 of IC4, which is applied to the varactor diode of the VCO to bring it precisely to 'on frequency.' An active low-pass filter (IC6) removes audible 1.5625kHz reference tone from the control voltage.

PLL Transmitter Test Points

Test point	Details
TP0, TP3	0V (GND)
TP1	+12V
TP2	Transmitted frequency
TP4	+5V
TP5	Frequency as set by DIP1-DIP4
TP6	1.5625kHz

Note: *All measurements are w.r.t. GND*

The reference frequency of the PLL is multiplied by the programmable divider divide rate to give the final frequency. If the divider rate is 1024 (as set by DIP switches DIP1-DIP4

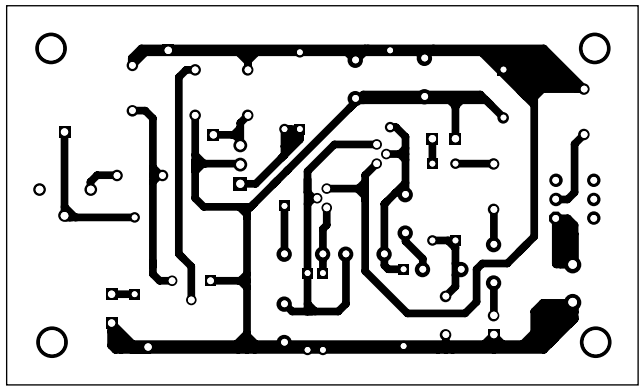

Fig. 3: Actual-size PCB layout of RF section

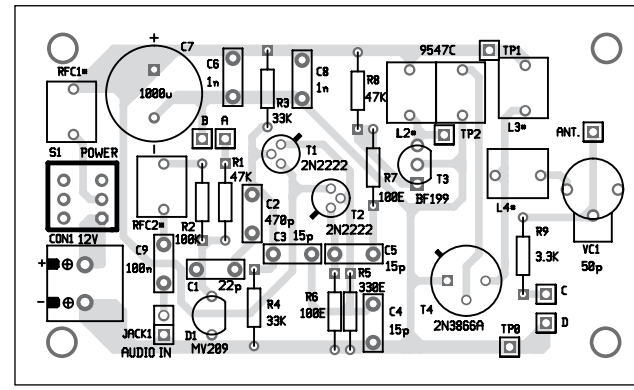

Fig. 4: Component layout of PCB of RF section

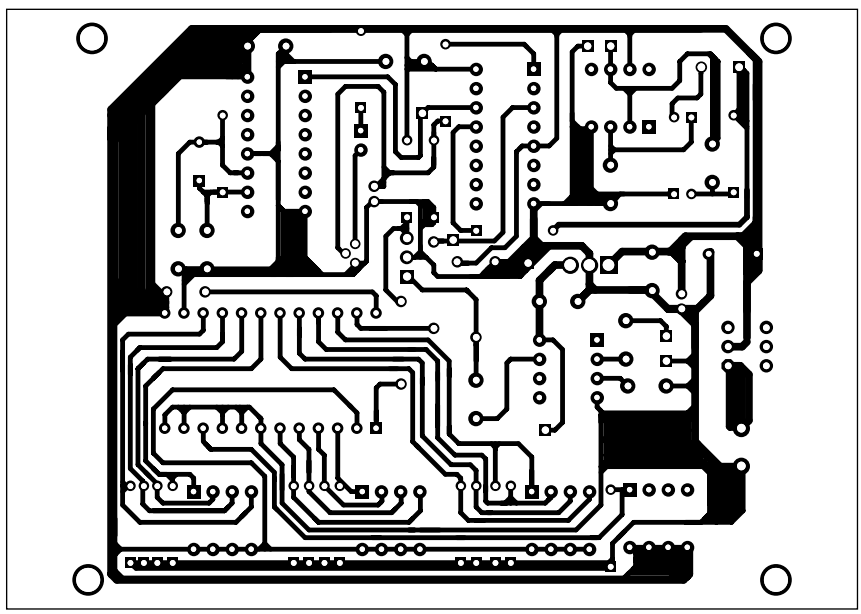

Fig. 5: Actual-size PCB layout of PLL control section

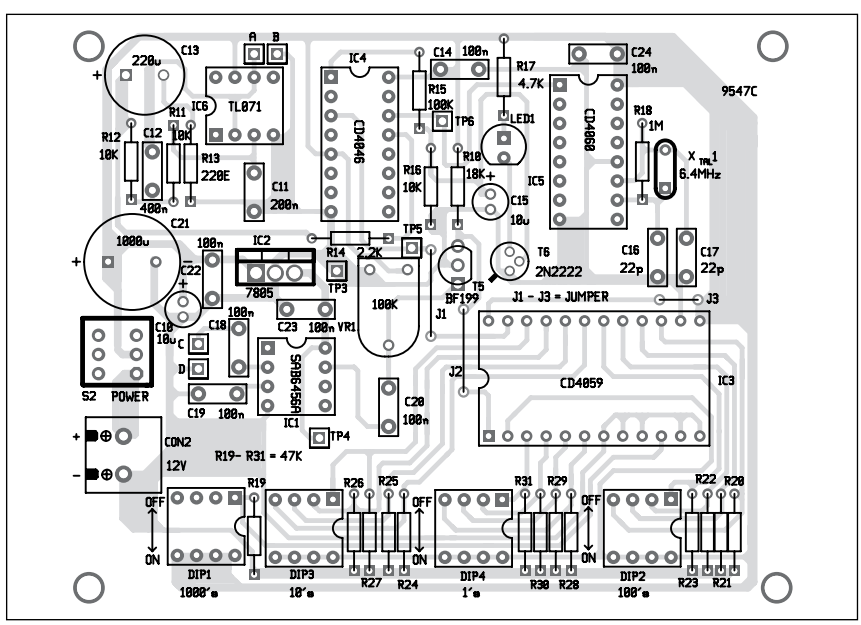

Fig. 6: Component layout of PCB of PLL control section

shown in Fig. 2), then the output will be 1.5625×1024×64 = 102.4MHz.

Similarly, a DIP setting of 1000 gives us an output frequency of 100MHz. LED1 lights up to indicate a lock on the selected frequency.

Construction and testing

An actual-size, single-layer PCB layout for Unit 1 is shown in Fig. 3 and its component layout in Fig. 4. Single-layer, actual-size PCB layout for Unit 2 is shown in Fig. 5 and its component layout in Fig. 6.

Assemble the circuits on the PCBs to save time and minimise assembly errors. Unit 1 is connected to Unit 2 by a co-axial cable of short length. Open end of resistor R1, indicated as 'A' in Unit 1, is connected to pin 6 of IC6, indicated as 'A' in Unit 2, by co-axial cable. Similarly, open end of resistor R9, indicated as 'C' in Unit 1, is connected to open end of C18, indicated as 'C' in Unit 2, by co-axial cable. Ground the shield wire of the coaxial cable.

Keep all leads as short as possible. To test the circuit for proper functioning, connect stabilised 12V supply to both the units. The circuit will accept audio signal from just about anything (CD, tape, iPod or computer) and transmit the signal, which can be received by an FM radio. An external microphone amplifier can be used for speech. A good matching 50-ohm ground-plane antenna will greatly enhance the range of transmission. Use appropriate IC bases on the PCB. ●

The author is an electronics hobbyist and a small-business owner in Albany, New York, USA. His interests include designing RF circuits