SONY

Cable Equalizer with 2-system Switching Function

CXB1441R

Description

The CXB1441R is a cable equalizer that compensates the attenuation resulting from cable transfer of small-amplitude differential NRZ signals.
This chip has two sets of input ports comprising three pairs of differential data signals and one pair of differential clock signals. It equalizes and quantizes the signals from the optional ports and then outputs the signal from the output ports. NRZ signals from 250Mb/s to 1.65Gb/s are supported.
(Applications: High-speed digital video signal switching and compensation of cable attenuation)

Features

- ◆ Two sets of input ports comprising three pairs of differential data signals and one pair of differential clock signals
- ◆ 50Ω termination pull-up resistors built into differential data and clock inputs
- ◆ Low differential data and clock input capacitance facilitates the design and manufacture of TDR standard compatible equipment
- ◆ Equalizer circuit that compensates cable attenuation improves the signal eye pattern
- ◆ Output 50Ω load drive, voltage amplitude 0.5Vp-p
- ◆ Single +3.3V power supply
- ◆ Low power consumption
- ◆ Lead-free 48-pin plastic LQFP package (7mm × 7mm)

Package

48-pin LQFP (Plastic)

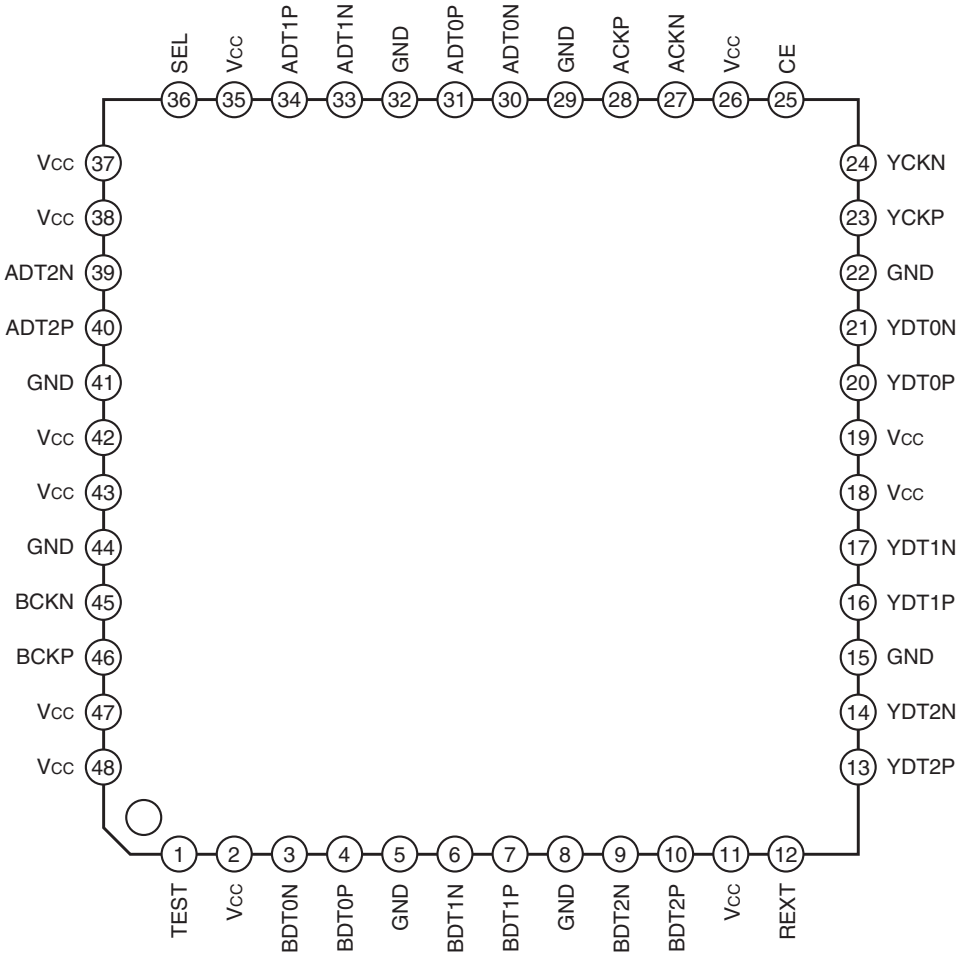
Absolute Maximum Ratings

◆ Supply voltage	V_{CC}	–0.3 to +4.0	V
◆ Storage temperature	Tstg	–65 to +150	˚C

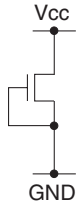
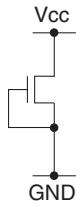
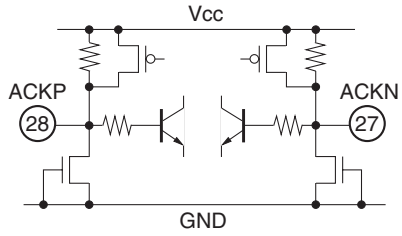
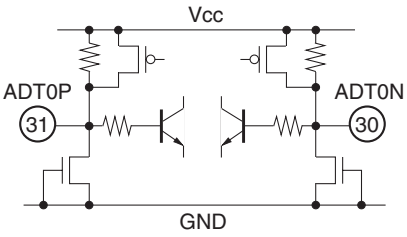
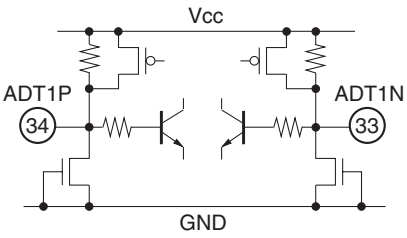
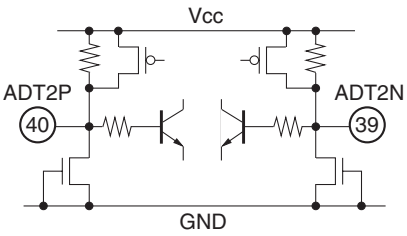
Recommended Operating Conditions

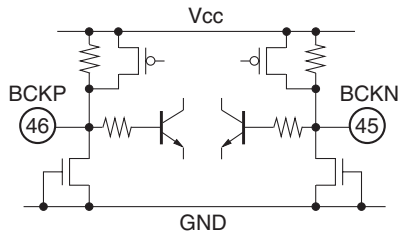
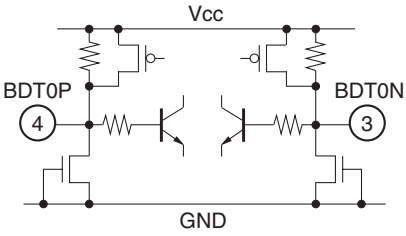
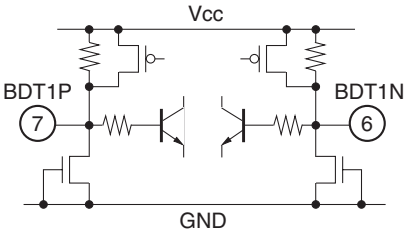
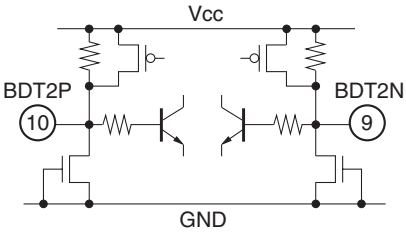
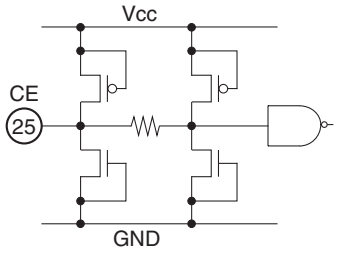
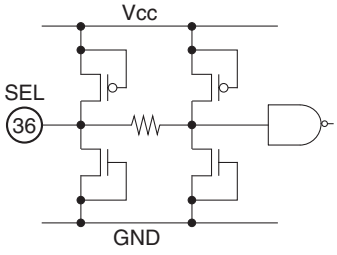
◆ Supply voltage	V_{CC}	3.135 to 3.465	V
◆ Operating temperature	Ta	–20 to +75	˚C

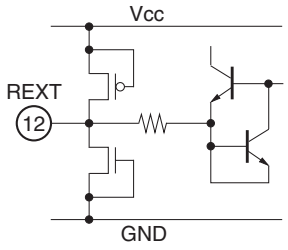
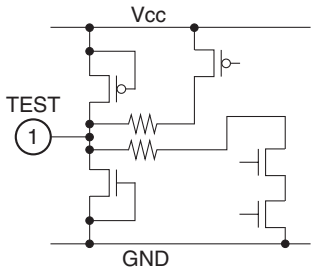
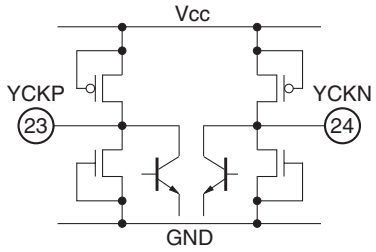
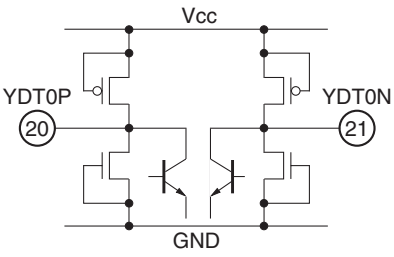
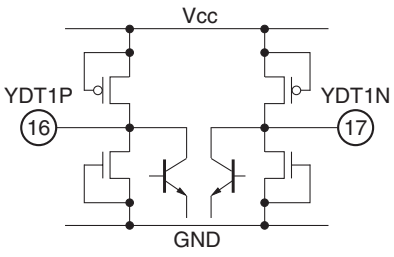
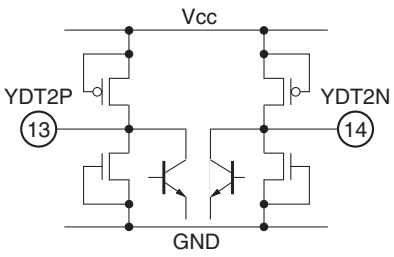
Pin Configuration



Pin Description

Pin No.	Symbol	Type	Equivalent circuit	Description
2, 11, 18, 19, 26, 35, 37, 38, 42, 43, 47, 48	VCC	Power supply		Power supply. Connect to 3.3V ± 5%.
5, 8, 15, 22, 29, 32, 41, 44	GND	GND		GND. Connect to 0V.
28	ACKP	Differential input		A port differential clock input.
27	ACKN			
31	ADT0P	Differential input		A port differential data input 0.
30	ADT0N			
34	ADT1P	Differential input		A port differential data input 1.
33	ADT1N			
40	ADT2P	Differential input		A port differential data input 2.
39	ADT2N			

Pin No.	Symbol	Type	Equivalent circuit	Description
46	BCKP	Differential input		B port differential clock input.
45	BCKN			
4	BDT0P	Differential input		B port differential data input 0.
3	BDT0N			
7	BDT1P	Differential input		B port differential data input 1.
6	BDT1N			
10	BDT2P	Differential input		B port differential data input 2.
9	BDT2N			
25	CE	CMOS in		Chip enabled by High input.
36	SEL	CMOS in		A ports selected by High input, B ports selected by Low input.

Pin No.	Symbol	Type	Equivalent circuit	Description
12	REXT	Analog		Connect to GND through a 4.7kΩ ± 1% input impedance adjusting resistor.
1	TEST	CMOS in		Test function control. Fix Low.
23	YCKP	Differential output		Differential clock output.
24	YCKN			
20	YDT0P	Differential output		Differential data output 0.
21	YDT0N			
16	YDT1P	Differential output		Differential data output 1.
17	YDT1N			
13	YDT2P	Differential output		Differential data output 2.
14	YDT2N			

Electrical Characteristics

DC characteristics

(Under the recommended operating conditions)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
CMOS input High level voltage	VIH_M	Vcc – 0.5		Vcc + 0.3	V	
CMOS input Low level voltage	VIL_M	–0.3		0.5	V	
CMOS input High level current	IIH_M			1	μA	@VIN = Vcc
CMOS input Low level current	IIL_M	–1			μA	@VIN = 0
Differential input pin resistance relative to Vcc	RTERM	45	50	55	Ω	@CE = Vcc, IIN = –10mA, *1
Differential input dynamic range	VI	Vcc – 0.8		Vcc + 0.2	V	
Differential output High level current	IOH	0		0.05	mA	
Differential output Low level current	IOL	8	10	12	mA	
Supply current (operating)	Icc	110		165	mA	CE = H, differential input open
Supply current (standby)	Istby			30	μA	CE = L, differential input open

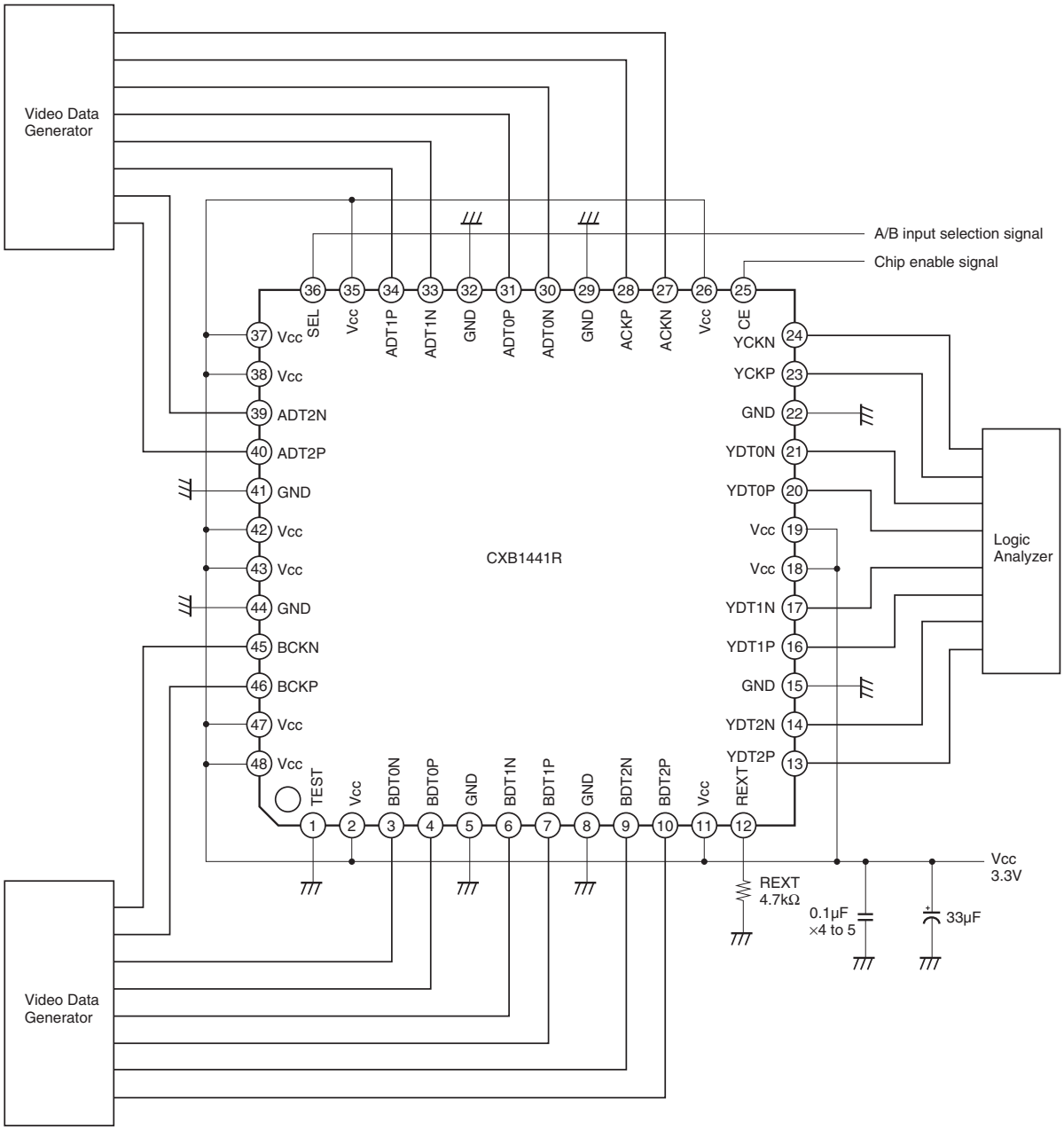
*1 The resistance value when CE = Low is 55Ω (typ.).

AC Characteristics

(Under the recommended operating conditions)

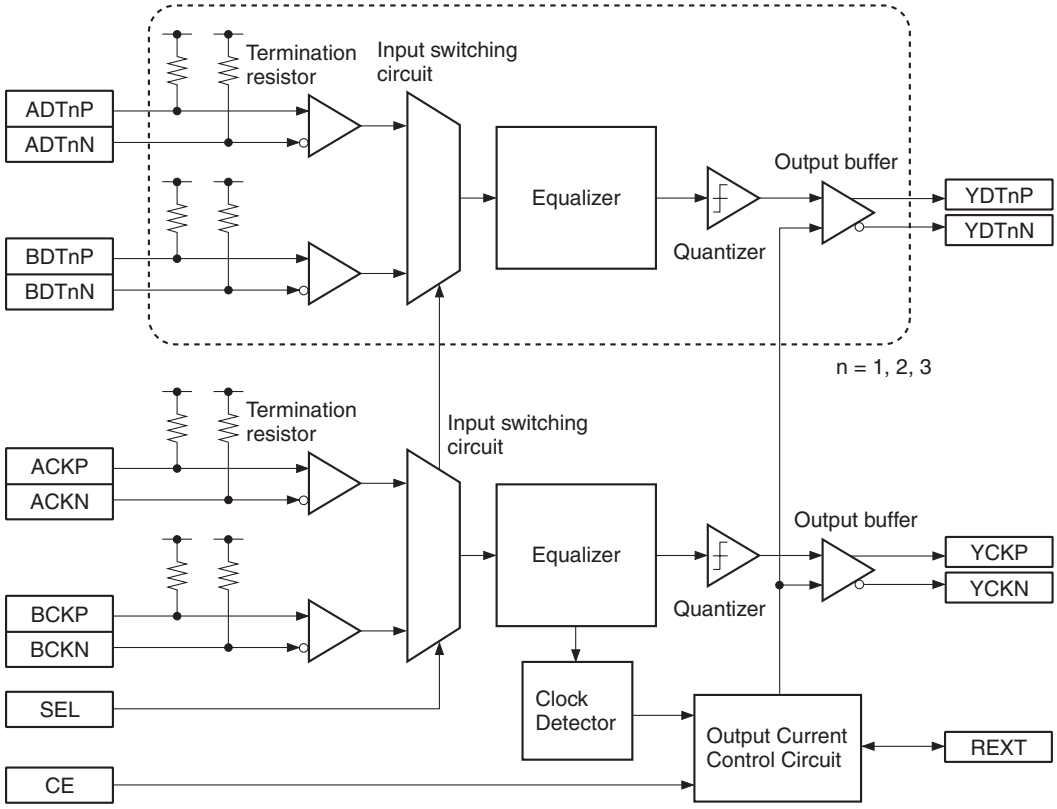
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock frequency	fCK	25		165	MHz	1/10 the differential data rate
Maximum equalizer gain	G_EQ	5			dB	@125MHz
		6			dB	@200MHz
		9			dB	@400MHz
		12			dB	@740MHz
Differential data and clock output rise/fall time	Tr		150		ns	20 to 80%
	Tf		150		ns	80 to 20%

Electrical Characteristics Measurement Circuit



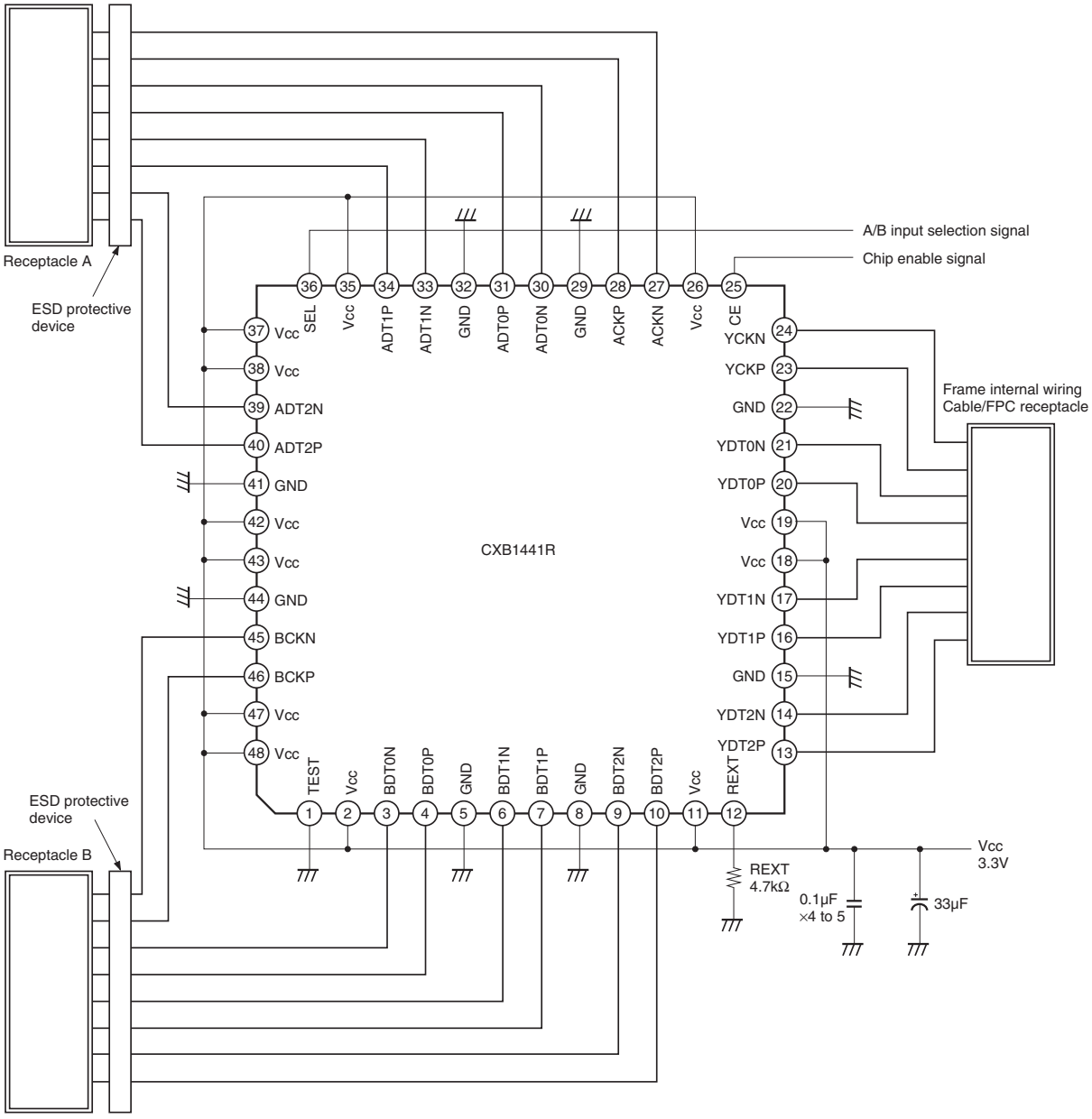
Description of Functions

The CXB1441R has two sets of input ports comprising three pairs of differential data signals and one pair of differential clock signals. The A ports are selected when a High signal is applied to the CMOS input pin SEL, and the B ports are selected when a Low signal is applied. Shaping is performed by the equalizer to compensate the signal deterioration of the selected port data signals and clock signals caused by transfer cable attenuation, and then these signals are quantized and reproduced on the output ports.
The CXB1441R inputs have built-in 50Ω pull-up resistors that act as transfer termination resistors, and parasitic capacitance is suppressed to a level that does not deteriorate the TDR characteristics of the equipment.
The outputs employ a 10mA differential current output format in order to drive external 50Ω pull-up resistors. This output current is driven only when a High signal is applied to the CMOS input pin CE and the clock signal of the selected input port is in differential mode.
When a Low signal is applied to the CMOS input pin CE, the CXB1441R enters standby mode to reduce the power consumption.
The CXB1441R can be controlled by operating only the CMOS input pins CE and SEL.



Function Block Diagram

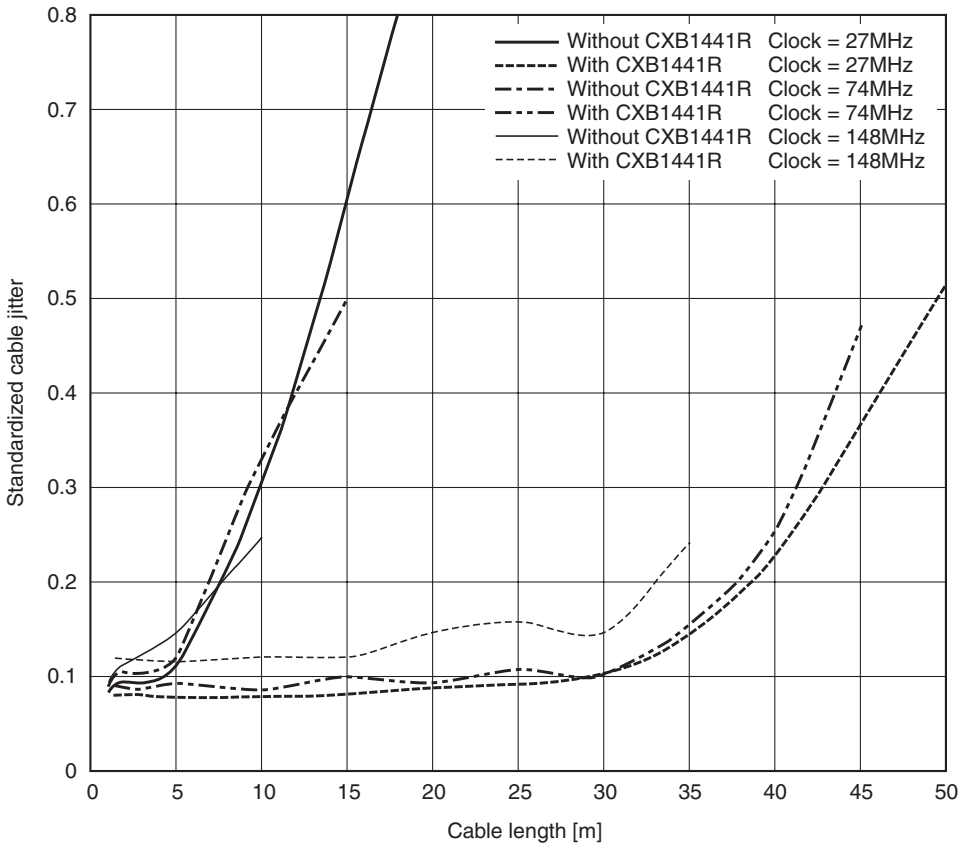
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Equalizer Characteristics

Example of cable jitter improvement effects



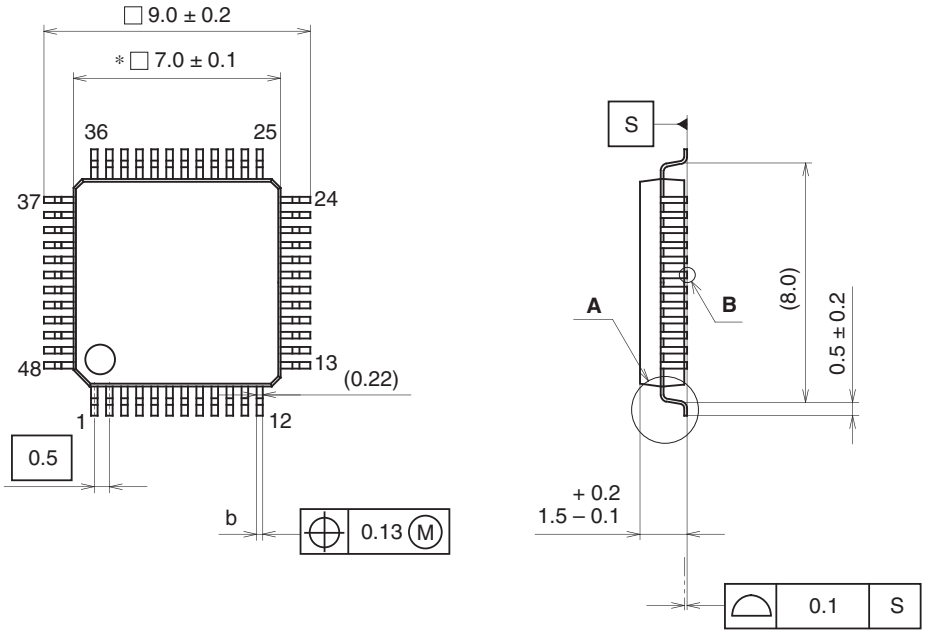
Notes On Handling

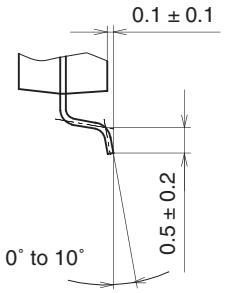
The guideline for cable attenuation that can be compensated by the equalizer is the maximum equalizer gain. However, this rule does not apply when skin effects cause the attenuation characteristics to deviate greatly from the square root of the frequency response, or for cables with a large skew.

Package Outline

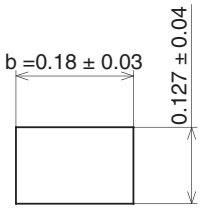
(Unit: mm)

48PIN LQFP (PLASTIC)





DETAIL **A**



DETAIL **B**: PALLADIUM

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	P-LQFP48-7x7-0.5
JEDEC CODE	————————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g