# Duobond Display Technology Co.,Ltd

# PRODUCT SPECIFICATION

MODEL NAME: TM034XDZP02

Date: 2018/08/05

Version: 1.0

■ **Preliminary Specification**

□ **Final Specification**

| | |
|---|---|
| FOR CUSTOMER | |
| CUSTOMER APPROVED | |

| PREPARED BY | CHECKED BY | APPROVED BY | DATE |
|---|---|---|---|
| | | | |

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# Record of Revision

| Rev | Issued Date | Description | Editor |
|---|---|---|---|
| 1.0 | 2018-07-13 | Preliminary Specification Release | Haiping_luo |
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# 1 General Specifications

| Feature | | Spec |
|---|---|---|
| **Display Spec.** | Size | 3.4 inch |
| | Resolution | 800(RGB)×800 |
| | Technology Type | a-Si |
| | Pixel Configuration | R.G.B. Vertical Stripe |
| | Pixel pitch(mm) | 0.1095×0.1095 |
| | Display Mode | SFT |
| | Surface Treatment | HC |
| | Viewing Direction | All direction |
| **Mechanical Characteristics** | LCM (W x H x D) (mm) | 96.6(W) x 99.0(H) x 2.45(D) |
| | LCD Active Area(mm) | 87.6(W) ×87.6 (H) |
| | Matching Connection Type | ZIF |
| | LED Numbers | 8 white LEDs |
| | Weight (g) | TBD |
| **Electrical Characteristics** | Interface | MIPI 3-Lane |
| | Color Depth | 16.7M |
| | Driver IC | ILI9881C |

Note 1: Viewing direction for best image quality is different from TFT definition. There is a 180 degree shift.

Note 2: Requirements on Environmental Protection: Q/S0002

Note 3: LCM weight tolerance: ± 5%

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# 2 Input/Output Terminals

## 2.1 LCM Interface Description

| Pin No. | Symbol | I/O | Function | Remark |
|---|---|---|---|---|
| 1 | GND | P | Ground | |
| 2 | LEDA | P | LED Anode | |
| 3 | LEDA | P | LED Anode | |
| 4 | LEDK | P | LED Cathode | |
| 5 | LEDK | P | LED Cathode | |
| 6 | GND | P | Ground | |
| 7 | VDD(-5V) | P | -5V INPUT | |
| 8 | VDD(-5V) | P | -5V INPUT | |
| 9 | GND | P | Ground | |
| 10 | VDD(+5V) | P | +5V INPUT | |
| 11 | VDD(+5V) | P | +5V INPUT | |
| 12 | GND | P | Ground | |
| 13 | IOVCC | P | Power supply 1.8V | |
| 14 | IOVCC | P | Power supply 1.8V | |
| 15 | GND | P | Ground | |
| 16 | RESET | I | Global Reset Pin | |
| 17 | GND | P | Ground | |
| 18 | TE | I | tearing effect output | |
| 19 | GND | P | Ground | |
| 20 | NC | / | No connect | |
| 21 | NC | / | No connect | |
| 22 | NC | / | No connect | |
| 23 | GND | P | Ground | |
| 24 | LAN2_P | I/O | MIPI lane 2+ | |
| 25 | NC | / | No connect | |
| 26 | LAN2_N | I/O | MIPI lane 2- | |
| 27 | GND | P | Ground | |
| 28 | CLK_P | I/O | MIPI clock + | |

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| | | | | |
|---|---|---|---|---|
| 29 | NC | / | No connect | |
| 30 | CLK_N | I/O | IMIPI clock - | |
| 31 | GND | P | Ground | |
| 32 | LAN1_P | I/O | MIPI lane 1+ | |
| 33 | NC | / | No connect | |
| 34 | LAN1_N | I/O | MIPI lane 1- | |
| 35 | GND | P | Ground | |
| 36 | LAN0_P | I/O | MIPI lane 0+ | |
| 37 | NC | / | No connect | |
| 38 | LAN0_N | I/O | MIPI lane 0- | |
| 39 | GND | P | Ground | |

# 3 Absolute Maximum Ratings

## 3.1 LCM absolute maximum reatings

GND=0V

| Item | Symbol | MIN | MAX | Unit | Remark |
|---|---|---|---|---|---|
| Power Supply Voltage | IOVCC | -0.3 | 3.3 | V | Note1 |
| Power Supply Voltage | VDD(+5V) | -0.3 | 6.5 | V | |
| Power Supply Voltage | VDD(-5V) | -6.5 | +0.3 | V | |
| Operating Temperature | Top | -20 | 70 | ℃ | |
| Storage Temperature | Tst | -30 | 80 | ℃ | |
| Relative Humidity Note2 | RH | -- | ≤95 | % | Ta≤40℃ |
| | | -- | ≤85 | % | 40℃＜Ta≤50℃ |
| | | -- | ≤55 | % | 50℃＜Ta≤60℃ |
| | | -- | ≤36 | % | 60℃＜Ta≤70℃ |
| | | -- | ≤24 | % | 70℃＜Ta≤80℃ |
| Absolute Humidity | AH | -- | ≤70 | g/m³ | Ta＞70℃ |

**Table 3 Absolute Maximum Ratings**

Note1: Input voltage include R0~R5, G0~G5, B0~B5, Dotclk, Hsync, Vsync, Enable, R/L, U/D.

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# 4 Electrical Characteristics

## 4.1 LCD electrical characteristics

GND=0V,Ta=25℃

| Item | | Symbol | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Logic operating voltage | | IOVCC | 1.7 | 1.8 | 1.9 | V | |
| Positive source output voltage | | VDD(+5V) | 4.9 | 5 | 5.1 | V | |
| Negative source output voltage | | VDD(-5V) | -5.1 | -5 | -4.9 | V | |
| Input Signal Voltage | High Level | VIH | 0.7*IOVCC | - | IOVCC | V | |
| | Low Level | VIL | 0 | - | 0.3*IOVCC | | |
| Output Voltage | High Level | $V_{OH}$ | 0.8 IOVCC | - | IOVCC | | |
| | Low Level | $V_{OL}$ | 0 | - | 0.2 IOVCC | | |

**Table 4.1 LCD module electrical characteristics**

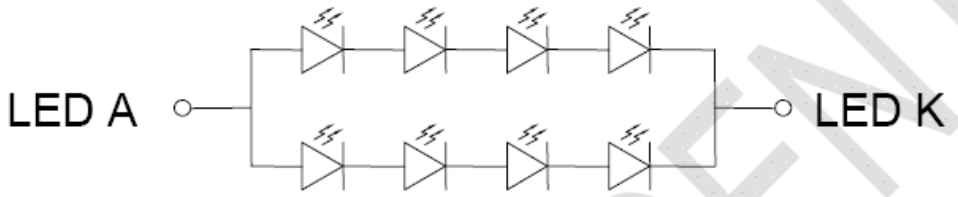
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### 4.4 Backlight Unit

Ta=25℃

| Item | Symbol | Min | Typ | Max | Unit | Remark |
|---|---|---|---|---|---|---|
| Forward Current | $I_F$ | - | 20 | - | mA | For each LED |
| Forward Voltage | $V_F$ | 2.9 | 3.2 | 3.4 | V | For each LED |
| Operating Life Time | - | - | 20,000 | - | Hrs | For each LED |

Note1: Figure below shows the connection of backlight LED.




LED CIRCUIT

(If=40mA / Vf=12.8V TYP)

Note 2: 1LED: $V_F$ =3.2V $I_F$ =20mA

Note 3: $I_F$ is defined for one LED.

Optical performance should be evaluated at Ta=25℃ only.

If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data

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# 5 Timing Chart

## 5.1 LCM Timing

### 5.1.1 Reset timing characteristics

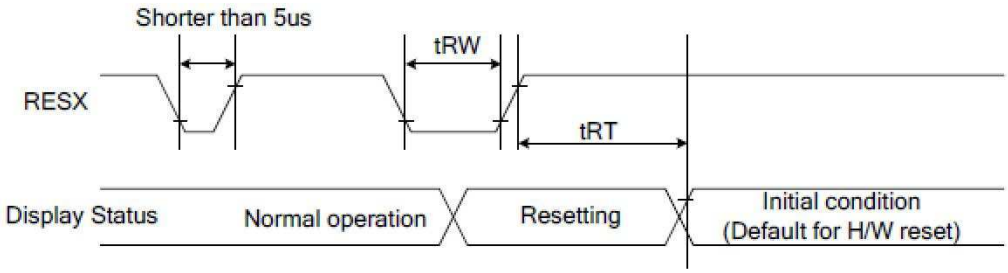



**Figure 124: Reset Timing**

**Table 47: Reset Timing**

| Signal | Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| RESX | tRW | Reset pulse duration | 10 | | uS |
| | tRT | Reset cancel | | 5 (note 1,5) | mS |
| | | | | 120 (note 1,6,7) | mS |

***Notes:***

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

**Table 48: Reset Descript**

| RESX Pulse | Action |
|---|---|
| Shorter than 5us | Reset Rejected |
| Longer than 10us | Reset |
| Between 5us and 10us | Reset starts |

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

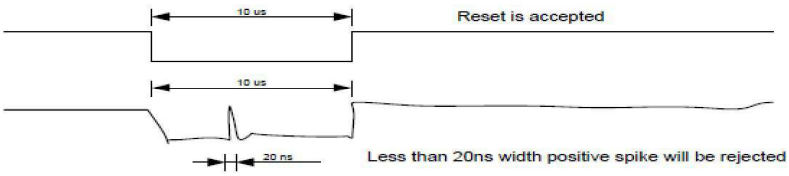



**Figure 125: Positive Noise Pulse during Reset Low**

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

### 5.1.2 High Speed Mode

#### 18.4.2. High Speed Mode – Clock Channel Timing

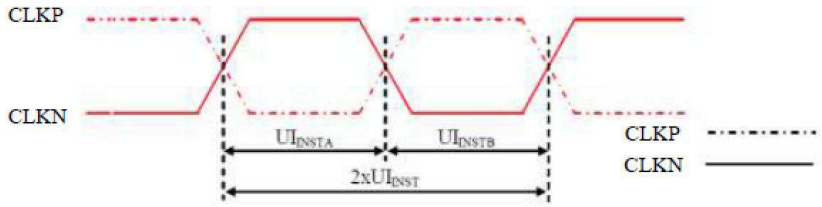



**Figure 116: DSI Clock Channel Timing**

**Table 38: DSI Clock Channel Timing**

| Signal | Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| CLKP/N | $2xUI_{INST}$ | Double UI instantaneous | *Note 2* | 25 | ns |
| CLKP/N | $UI_{INSTA}$, $UI_{INSTB}$ (Note 1) | UI instantaneous Half | *Note 2* | 12.5 | ns |

***Notes:***

*1. UI = UIINSTA = UIINSTB*

*2. Define the minimum value, see Table 39.*

**Table 39: Limited Clock Channel Speed**

| Data type | Two Lanes speed | Three Lanes speed | Four Lanes speed |
|---|---|---|---|
| Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel | 566 Mbps | 466 Mbps | 366 Mbps |
| Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel | 637 Mbps | 525 Mbps | 412 Mbps |
| Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel | 850 Mbps | 700 Mbps | 550 Mbps |
| Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel | 850 Mbps | 700 Mbps | 550 Mbps |

#### 18.4.3. High Speed Mode – Data Clock Channel Timing

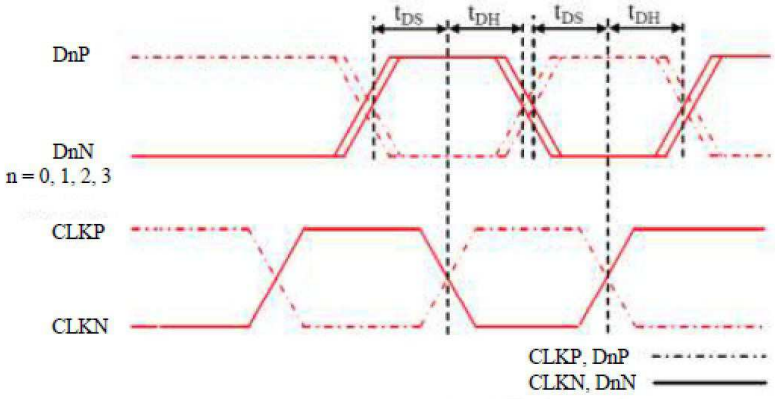



**Figure 117: DSI Data to Clock Channel Timings**

**Table 40: DSI Data to Clock Channel Timings**

| Signal | Symbol | Parameter | Min | Max |
|---|---|---|---|---|
| DnP/N , n=0 and 1 | $t_{DS}$ | Data to Clock Setup time | 0.15xUI | - |
| | $t_{DH}$ | Clock to Data Hold Time | 0.15xUI | - |

### 18.4.4. High Speed Mode – Rising and Falling Timings

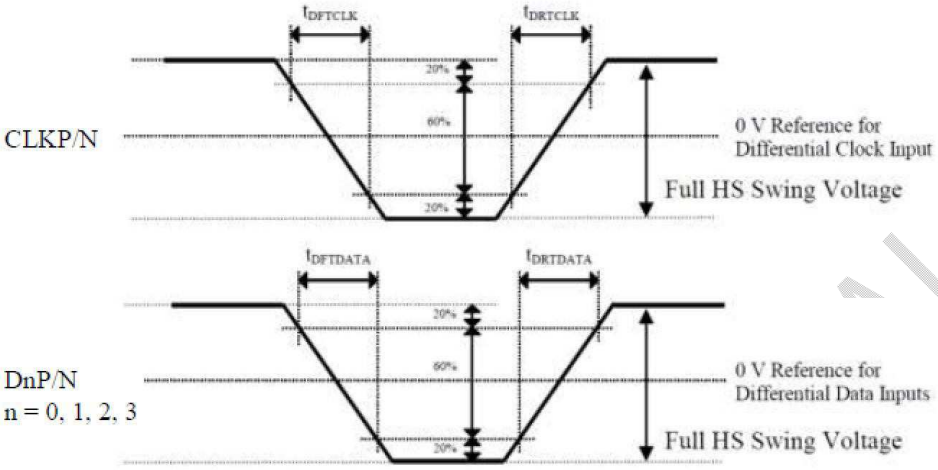



**Figure 118: Rising and Falling Timings on Clock and Data Channels**

**Table 41: Rise and Fall Timings on Clock and Data Channels**

| Parameter | Symbol | Condition | Specification | | |
|---|---|---|---|---|---|
| | | | Min | Typ | Max |
| Differential Rise Time for Clock | $t_{DRTCLK}$ | CLKP/N | 150 ps | - | 0.3UI (Note) |
| Differential Rise Time for Data | $t_{DRTDATA}$ | DnP/N n=0 and 1 | 150 ps | - | 0.3UI (Note) |
| Differential Fall Time for Clock | $t_{DFTCLK}$ | CLKP/N | 150 ps | - | 0.3UI (Note) |
| Differential Fall Time for Data | $t_{DFTDATA}$ | DnP/N n=0 and 1 | 150 ps | - | 0.3UI (Note) |

***Note:*** *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

### 5.1.3 Low Speed Mode

#### 18.4.5. Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

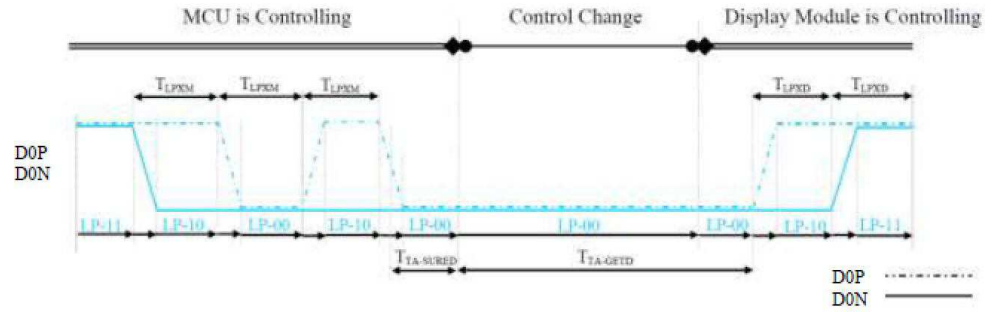



**Figure 119: BTA from the MCU to the Display Module**

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.

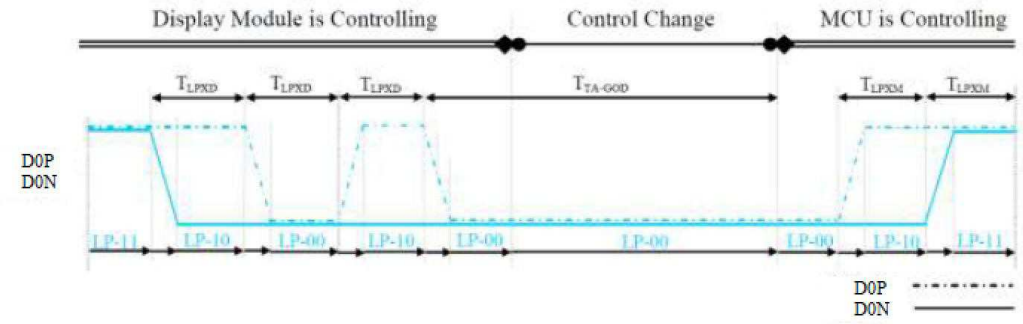



**Figure 120: BTA from the Display Module to the MCU**

**Table 42: Low Power State Period Timings – A**

| Signal | Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|---|
| D0P/N | $T_{LPXM}$ | Length of LP-00, LP-01, LP-10 or LP-11 periods<br>MCU → Display Module (ILI9881C) | 50 | 75 | ns |
| D0P/N | $T_{LPXD}$ | Length of LP-00, LP-01, LP-10 or LP-11 periods<br>Display Module (ILI9881C) → MCU | 50 | 75 | ns |
| D0P/N | $T_{TA-SURED}$ | Time-out before the Display Module (ILI9881C) starts driving | $T_{LPXD}$ | $2xT_{LPXD}$ | ns |

**Table 43: Low Power State Period Timings – B**

| Signal | Symbol | Description | Time | Unit |
|---|---|---|---|---|
| D0P/N | $T_{TA-GETD}$ | Time to drive LP-00 by Display Module (ILI9881C) | $5xT_{LPXD}$ | ns |
| D0P/N | $T_{TA-GOD}$ | Time to drive LP-00 after turnaround request - MCU | $4xT_{LPXD}$ | ns |

### 18.4.6. Data Lanes from Low Power Mode to High Speed Mode

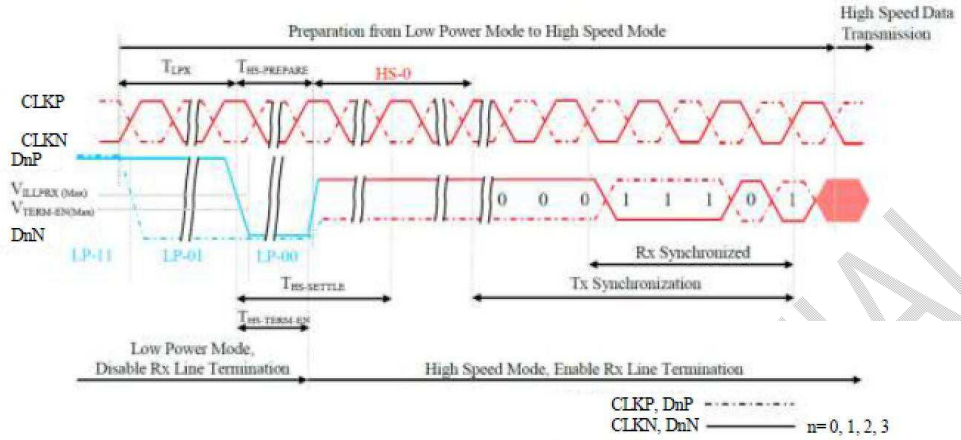



**Figure 121: Data Lanes - Low Power Mode to High Speed Mode Timings**

**Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings**

| Signal | Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|---|
| DnP/N, n = 0 and 1 | $T_{LPX}$ | Length of any Low Power State Period | 50 | - | ns |
| DnP/N, n = 0 and 1 | $T_{HS-PREPARE}$ | Time to drive LP-00 to prepare for HS Transmission | 40+4xUI | 85+6xUI | ns |
| DnP/N, n = 0 and 1 | $T_{HS-TERM-EN}$ | Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX | - | 35+4xUI | ns |

### 18.4.7. Data Lanes from High Speed Mode to Low Power Mode

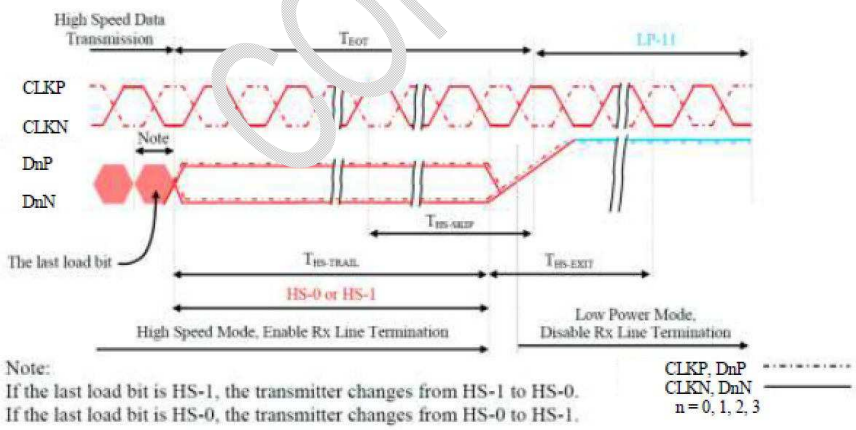
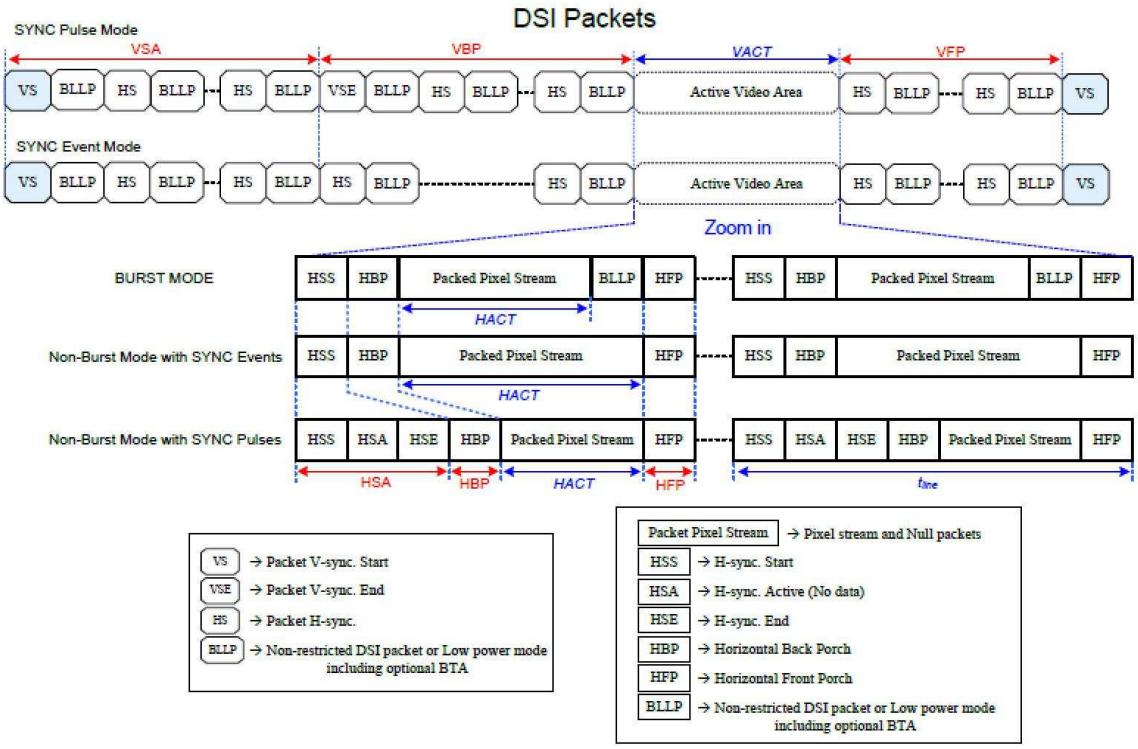



**Figure 122: Data Lanes - High Speed Mode to Low Power Mode Timings**

**Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings**

| Signal | Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|---|
| DnP/N, n = 0 and 1 | $T_{HS-SKIP}$ | Time-Out at Display Module (ILI9881C) to ignore transition period of EoT | 40 | 55+4xUI | ns |
| DnP/N, n = 0 and 1 | $T_{HS-EXIT}$ | Time to driver LP-11 after HS burst | 100 | - | ns |

### 18.4.9. Timing for DSI video mode




| Parameters | Symbols | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Vertical sync. active | VSA | 2 (Note 6) | - | - | Line |
| Vertical Back Porch | VBP | 14 (Note 6) | - | - | Line |
| Vertical Front Porch | VFP | 8 (Note 6) | - | - | Line |
| Active lines per frame | VACT | - | 1280 | - | Line |
| Horizontal sync. active | HSA | 2 | - | - | Pixel |
| Horizontal Porch period | HSA + HBP + HFP | 1.6 | - | - | us |
| Active pixels per line | HACT | - | 720 | - | Pixel |
| Bit rate | $BR_{bps}$ | 385 | | Note 5 | Mbps/lane |

1 UI=1/Bit rate

HSA(pixel)= (tHSA*lane number ) / (UI* pixel format )

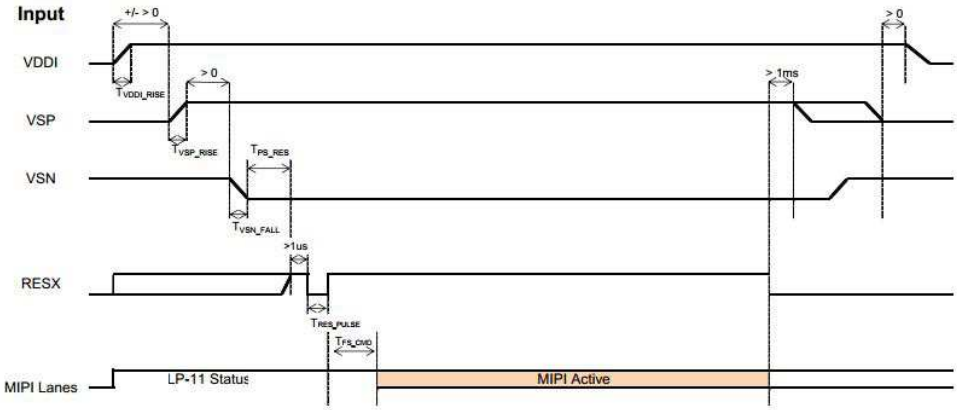
HBP(pixel)= (tHBP*lane number ) / (UI* pixel format )

HFP(pixel)= (tHFP*lane number ) / (UI* pixel format )

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example : $BR_{bps}$ = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, $Lane_{num}$=4(lane), Pixel Format=24(bit).

### 5.1.4 POWER ON/OFF SEQUENCE




| Symbol | Characteristics | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $T_{VDDI_RISE}$ | VDDI Rise time | 10 | - | - | us |
| $T_{VSP_RISE}$ | VSP Rise time | 130 | - | - | us |
| $T_{VSN_FALL}$ | VSN Fall time | 200 | - | - | us |
| $T_{PS_RES}$ | VDDI/VSP on to Reset high | 5 | - | - | ms |
| $T_{RES_PULSE}$ | Reset low pulse time | 10 | - | - | us |
| $T_{FS_CMD}$ | Reset to first command | 10 | - | - | ms |

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## 6 Optical Characteristics

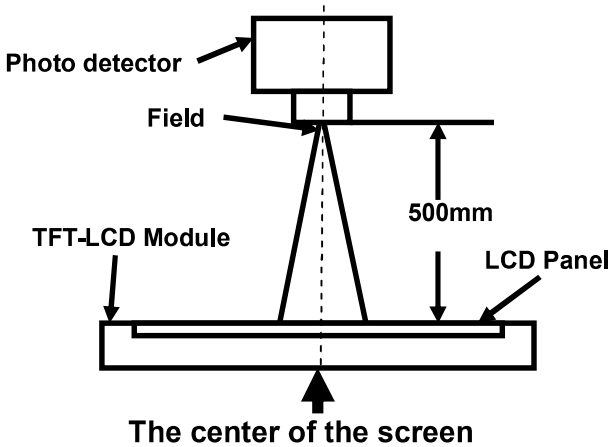
| Item | | Symbol | Condition | Min | Typ | Max | Unit | Remark |
|---|---|---|---|---|---|---|---|---|
| View Angles | | θT | CR≧10 | 70 | 80 | - | Degree | Note2 |
| | | θB | | 70 | 80 | - | | |
| | | θL | | 70 | 80 | - | | |
| | | θR | | 70 | 80 | - | | |
| Contrast Ratio | | CR | θ=0° | 600 | 800 | - | | Note 3 |
| Chromaticity | White | x | Backlight is on | 0.255 | 0.295 | 0.335 | | Note 1,5 |
| | | y | | 0.282 | 0.322 | 0.362 | | |
| Uniformity | | U | | 75 | 80 | - | % | Note 6 |
| Response Time | | Ton+Toff | - | - | 25 | 35 | | Note 1,4 |
| NTSC | | - | - | 65 | 70 | - | % | Note 5 |
| Luminance | | L | - | 300 | 380 | - | $cd/m^2$ | Note 7 |

Test Conditions:

1. $I_F$= 20 mA(one LED), and the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.

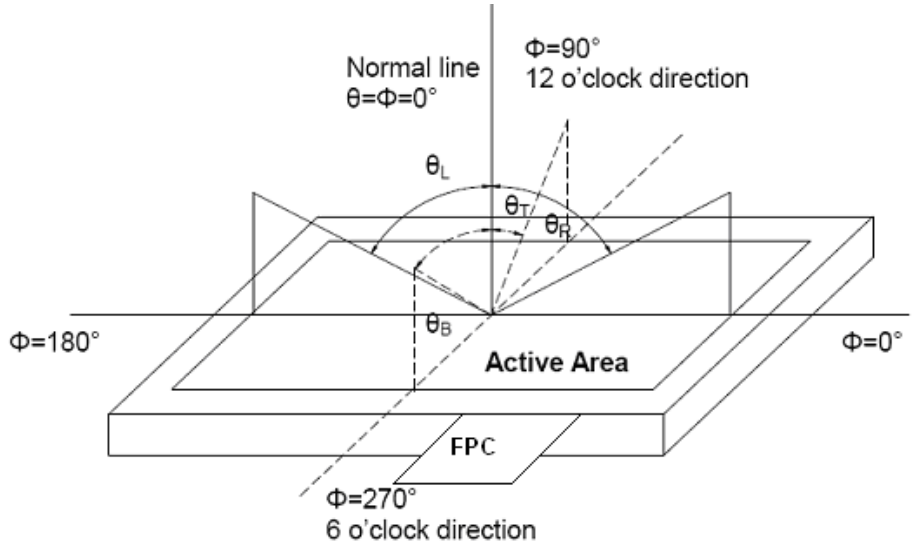
The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.




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Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD




Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

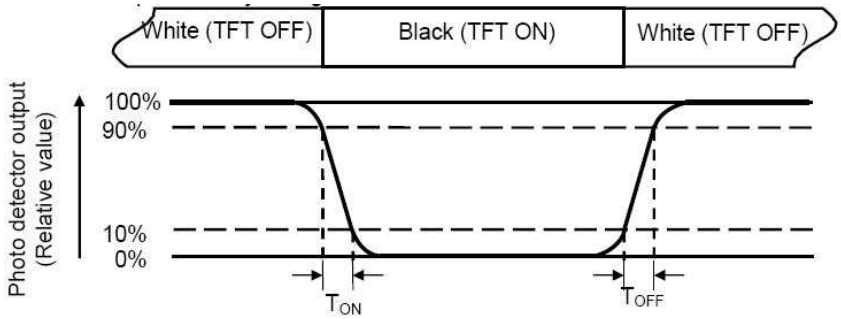
"White state ": The state is that the LCD should drive by Vwhite.

"Black state": The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time ($T_{ON}$) is the time between photo detector output intensity changed from 90% to 10%. And fall time ($T_{OFF}$) is the time between photo detector output intensity changed from 10% to 90%.




Note 5: Definition of color chromaticity (CIE1931)

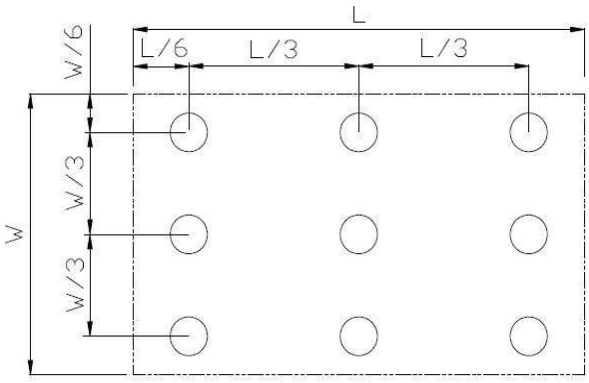
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L--------Active area length W------ Active area width




Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance: Measure the luminance of white state at center point.

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# 7 Environmental / Reliability Test

## 7.1 LCM+CTP

| No | Test Item | Condition | Remarks |
|---|---|---|---|
| 1 | High Temperature Operation | Ts=+70℃±2℃, 120hrs | IEC60068-2-1:2007 GB2423.2-2008 |
| 2 | Low Temperature Operation | Ta=-20℃±2℃, 120hrs | IEC60068-2-1:2007 GB2423.1-2008 |
| 3 | High Temperature Storage | Ta=+80℃±2℃, 120hrs | IEC60068-2-1:2007 GB2423.2-2008 |
| 4 | Low Temperature Storage | Ta=-30℃±2℃, 120hrs | IEC60068-2-1:2007 GB2423.1-2008 |
| 5 | Storage at High Temperature and Humidity | Ta=+60℃, 90% RH, 120hrs | IEC60068-2-78 :2001 GB/T2423.3—2006 |
| 6 | Thermal Shock (non-operation) | (-30℃/30min~80℃/30min)*20 cycles<br>Change Speed: 8℃/min | Start with cold temperature, End with high temperature, IEC60068-2-14:1984,GB2423.22-2002 |
| 7 | Electro Static Discharge (operation) | C=150pF R=330Ω Air: ±8KV Contact:±4KV 5point/panel, 5times | IEC61000-4-2:2001 GB/T17626.2-2006 |

Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of sample.

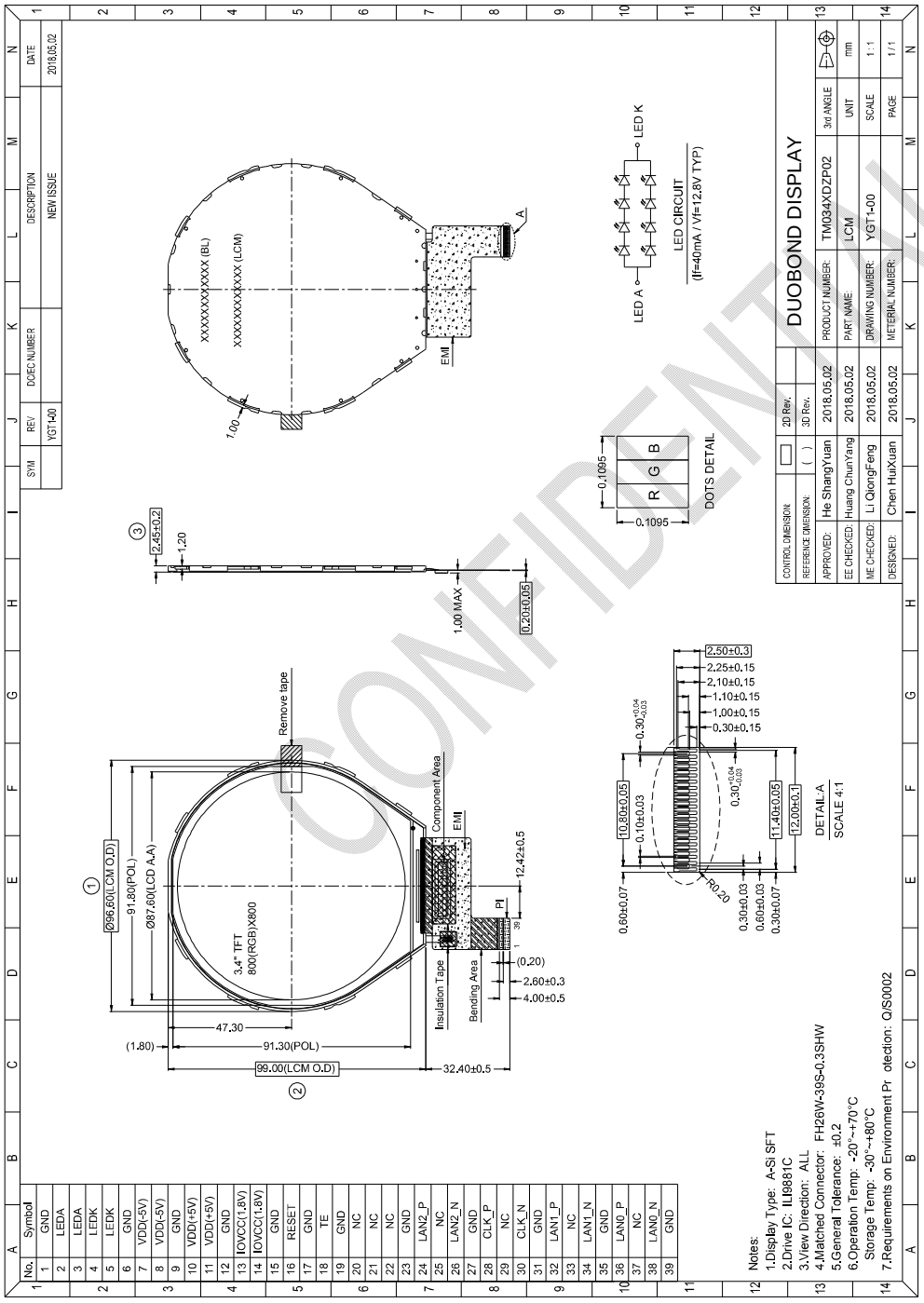
Note3: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

Note 4: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

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# 8 Mechanical Drawing

## 8.1 LCM+CTP Drawing




| No. | Symbol |
|---|---|
| 1 | GND |
| 2 | LEDA |
| 3 | LEDA |
| 4 | LEDK |
| 5 | LEDK |
| 6 | GND |
| 7 | VDD(-5V) |
| 8 | VDD(-5V) |
| 9 | GND |
| 10 | VDD(+5V) |
| 11 | VDD(+5V) |
| 12 | GND |
| 13 | IOVCC(1.8V) |
| 14 | IOVCC(1.8V) |
| 15 | GND |
| 16 | RESET |
| 17 | GND |
| 18 | TE |
| 19 | GND |
| 20 | NC |
| 21 | NC |
| 22 | NC |
| 23 | GND |
| 24 | LAN2_P |
| 25 | NC |
| 26 | LAN2_N |
| 27 | GND |
| 28 | CLK_P |
| 29 | NC |
| 30 | CLK_N |
| 31 | GND |
| 32 | LAN1_P |
| 33 | NC |
| 34 | LAN1_N |
| 35 | GND |
| 36 | LAN0_P |
| 37 | NC |
| 38 | LAN0_N |
| 39 | GND |

# 9 Packing Drawing

## 9.1 Per Carton

| No | Item | Model (Materiel) | Dimensions(mm) | Unit Weight(Kg) | Quantity | Remark |
|---|---|---|---|---|---|---|
| 1 | LCM module | | 96.6×99.0×2.45 | TBD | 112 | |
| 2 | Tray | | 356x256x12 | TBD | 30 | |
| 3 | EPE（珍珠棉1) | | 312.67×216×1 | TBD | 28 | |
| 4 | EPE（珍珠棉2） | MBZ-ZZML9 | 336×246×8 | TBD | 4 | |
| 5 | EPE（珍珠棉3） | MBZ-ZZM15 | 375×275×10 | TBD | 4 | |
| 6 | EPE（珍珠棉4） | MBZ-ZZM16 | 250×280×12 | TBD | 2 | |
| 7 | Carton（纸箱） | X18A | 395×290×315 | TBD | 1 | |
| 8 | Total weight | TBD | | | | |

## 9.2 Packaging Specification and Quantity

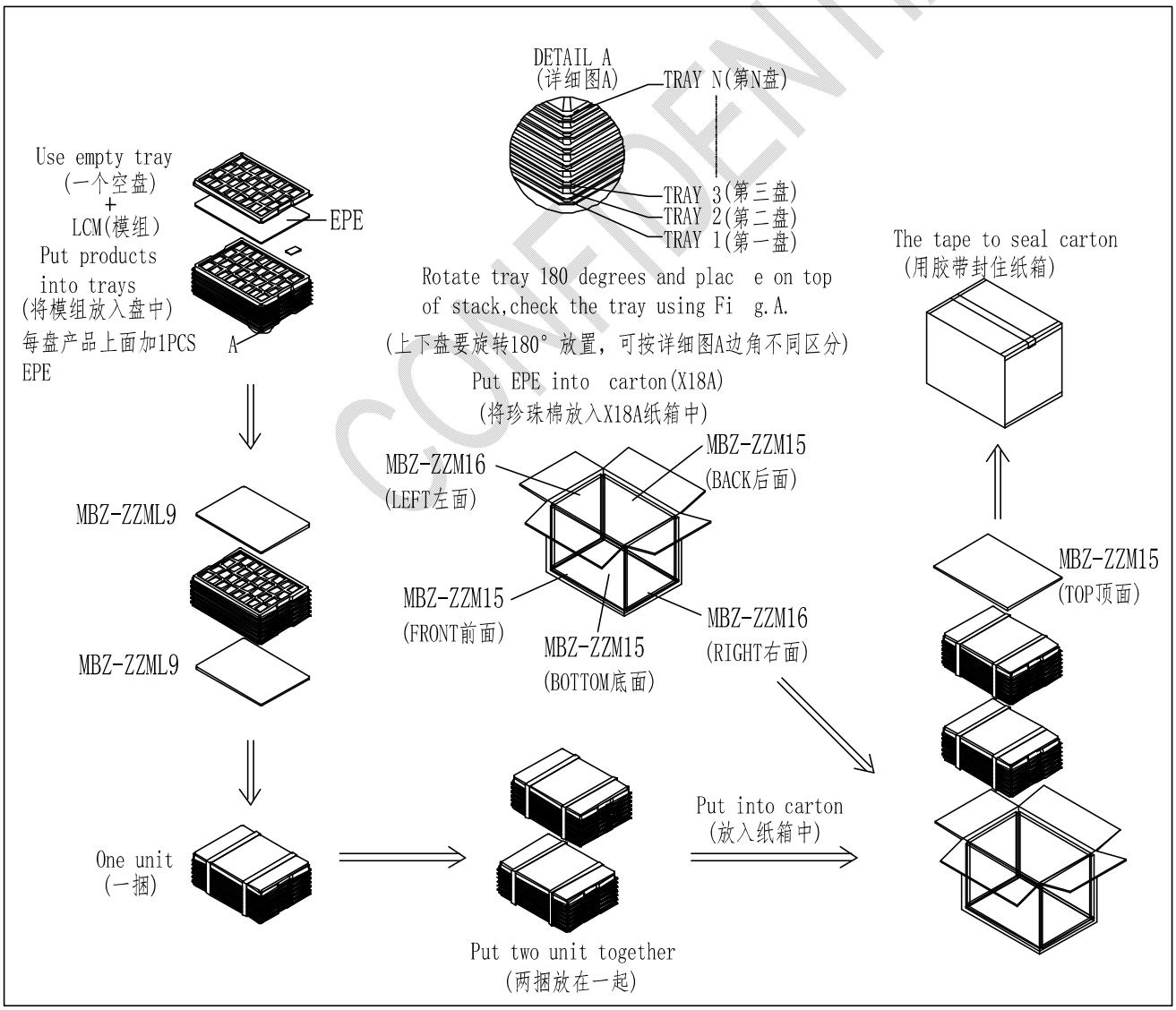
| |
|---|
| (1) LCM quantity per tray（每盘模组数量）:4 pcs |
| (2) Total LCM quantity per group（每组模组总数量）：56 pcs（14Tray盘+1 Enpty tray空盘） |
| (3) Total LCM quantity per Carton（每箱模组总数量）：quantity per group（每组模组总数量）56 pcs× group quantity per Carton（每箱组数量）2= 112 pcs |

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### 9.3 LCM 喷码规格

| | |
|---|---|
| 喷码位置 | 背光源背面 |
| 喷码内容 | 第一行:厂别　模块型号　生产日期 |
| | 第二行:　投产单号　班别 |
| 备注 | 生产日期格式为年月日（YYMMDD） |

### 9.4 Packing Form




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# 10 Precautions for Use of LCD Modules

10.1 Handling Precautions

10.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5 If the display surface is contaMinated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

10.1.6 Do not attempt to disassemble the LCD Module.

10.1.7 If the logic circuit power is off, do not apply the input signals.

10.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

13.1.8.1 Be sure to ground the body when handling the LCD Modules.

13.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

13.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

3.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage precautions

10.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

10.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

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10.3.1 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

10.3.2 About the limited warranty unless special agreement between and customer will replace or repair any of its products that are found to be functionally defective when inspected in accordance withTIANMA acceptance standards for a period of one yearfrom data of shipments. 除 跟客户签定协议外，对确认为属于产品本身功能性缺陷的，在 可接受范围内可进行退换或维修， 保质期为从出货日期起一年内有效。

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