INTEL

NIOS II Hello WORLD

QUARTUS 18.1

Nikki

01.08.2019

Question:

Why doesnt the NIOS II Console show Hello World !

(Also see Attachment)

Version 0

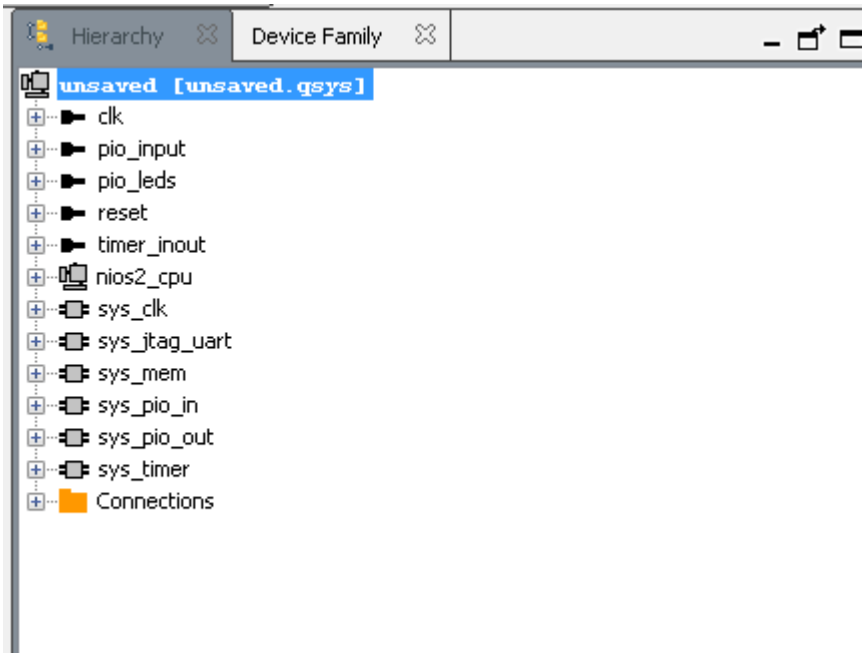


FIGURE 1 IPS

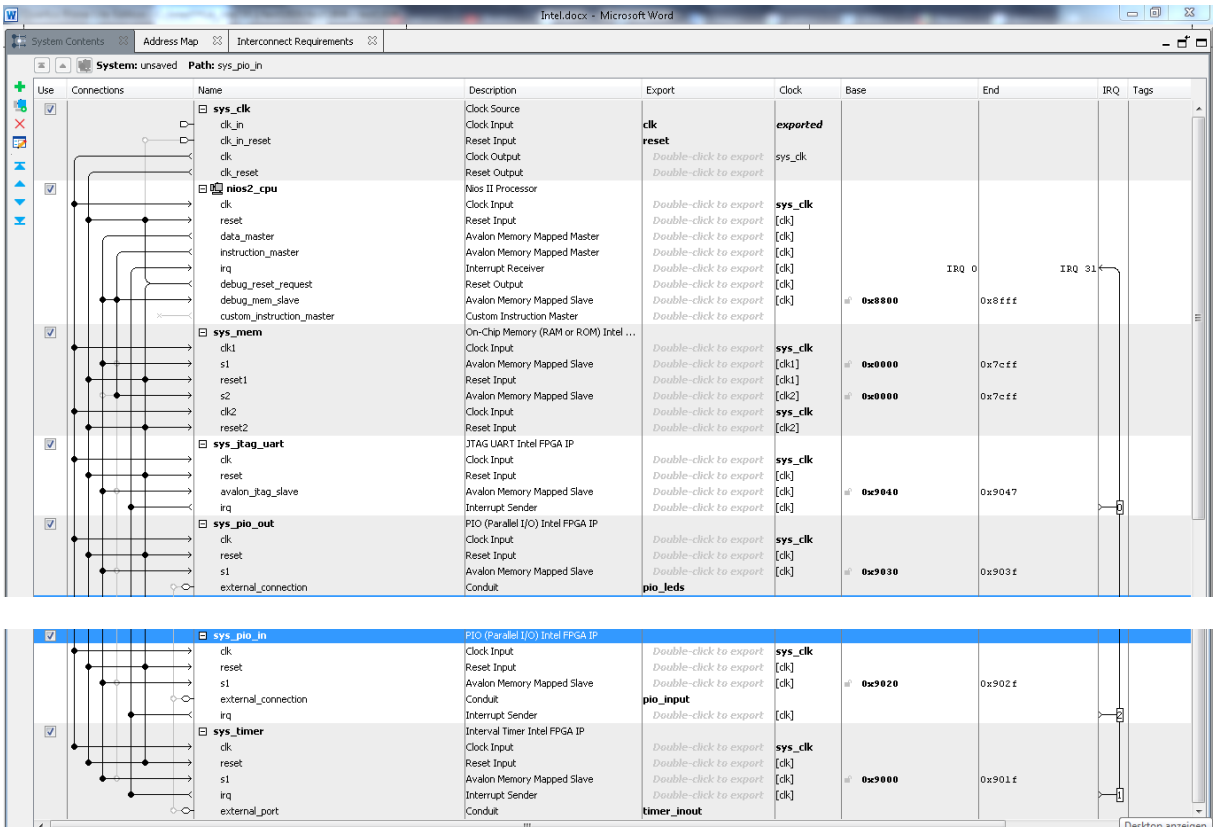


FIGURE 2 IPS

System Contents | Address Map | Interconnect Requirements

System: unsaved **Path:** sys_clk

	nios2_cpu.data_master	nios2_cpu.instruction_master
nios2_cpu.debug_mem_slave	0x8800 - 0x8fff	0x8800 - 0x8fff
sys_jtag_uart.avalon_jtag_slave	0x9040 - 0x9047	
sys_mem.s1	0x0000 - 0x7cff	
sys_mem.s2		0x0000 - 0x7cff
sys_pio_in.s1	0x9020 - 0x902f	
sys_pio_out.s1	0x9030 - 0x903f	
sys_timer.s1	0x9000 - 0x901f	

Nios II Processor

altera_nios2_gen2

Main | Vectors | Caches and Memory Interfaces | Arithmetic Instructions | MMU and MPU Settings | JTAG Debug | Advanced Features

Select an Implementation

Nios II Core: ○ Nios II/e ◉ Nios II/f

	Nios II/e	Nios II/f
Summary	**Resource-optimized 32-bit RISC**	**Performance-optimized 32-bit RISC**
Features	**JTAG Debug** **ECC RAM Protection**	**JTAG Debug** **Hardware Multiply/Divide** **Instruction/Data Caches** **Tightly-Coupled Masters** **ECC RAM Protection** **External Interrupt Controller** **Shadow Register Sets** **MPU** **MMU**
RAM Usage	2 + Options	2 + Options

Nios II Processor

altera_nios2_gen2

Main | Vectors | Caches and Memory Interfaces | Arithmetic Instructions | MMU and MPU Settings | JTAG Debug | Advanced Features

Reset Vector

Reset vector memory: sys_mem.s2

Reset vector offset: 0x00000000

Reset vector: 0x00000000

Exception Vector

Exception vector memory: sys_mem.s2

Exception vector offset: 0x00000020

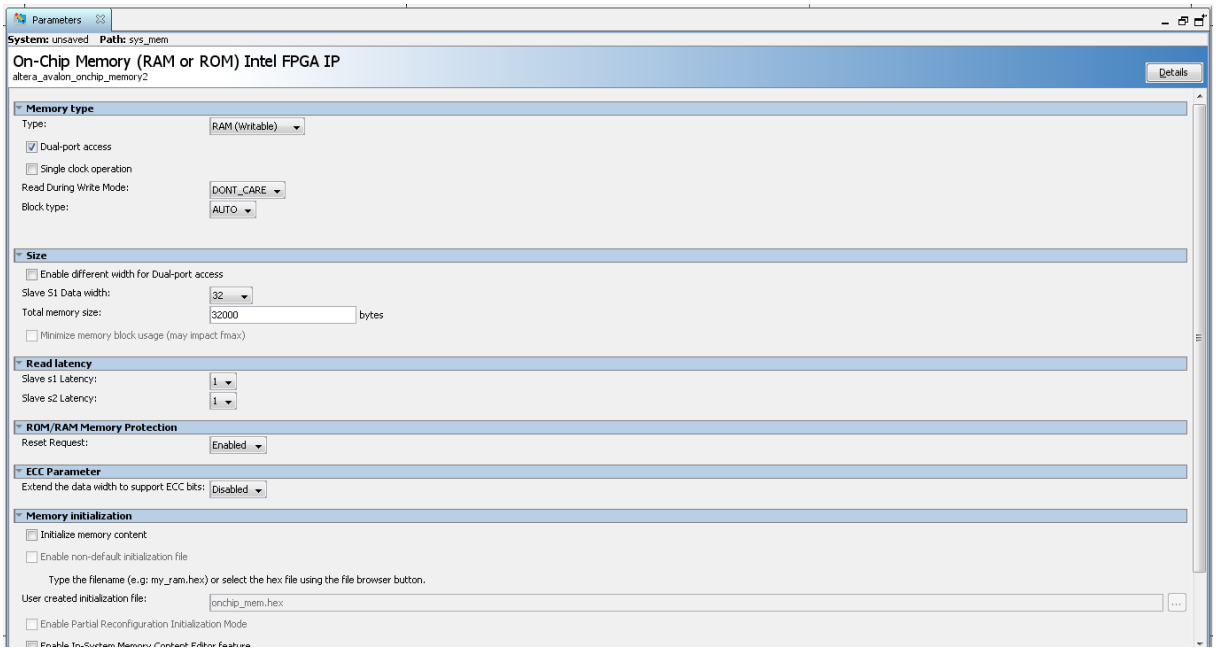
Exception vector: 0x00000020

Fast TLB Miss Exception Vector

Fast TLB Miss Exception vector memory: None

Fast TLB Miss Exception vector offset: 0x00000000

Fast TLB Miss Exception vector: 0x00000000



Configure interconnect requirements for the system or an interface.

System-wide Requirements

Limit interconnect pipeline stages to: 1

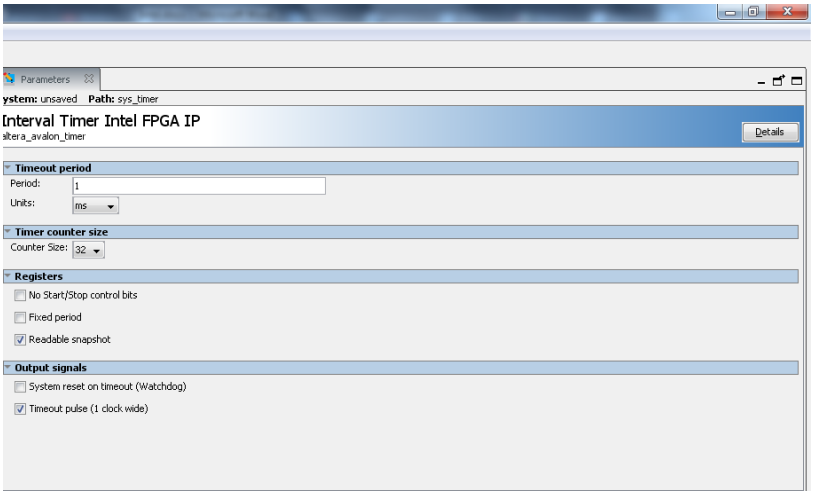
Clock crossing adapter type: Handshake

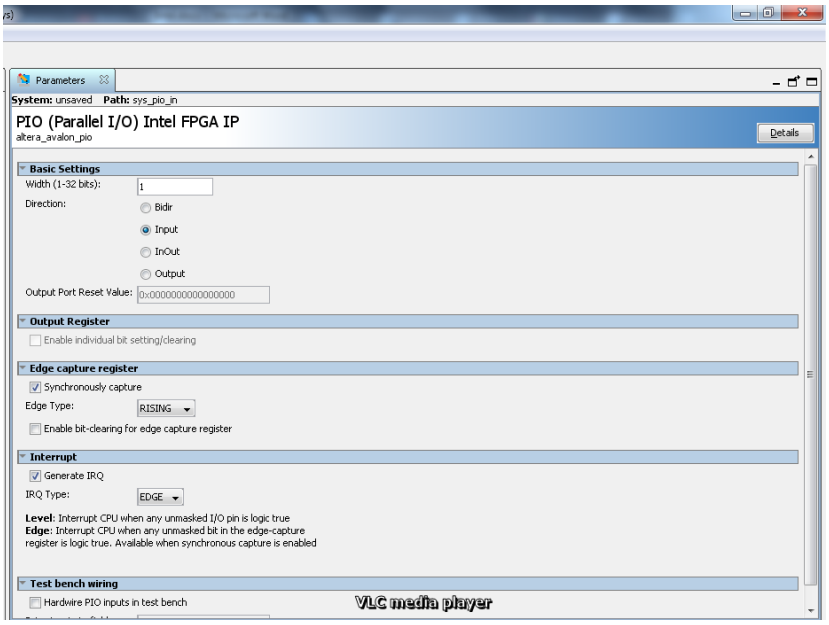
All Requirements

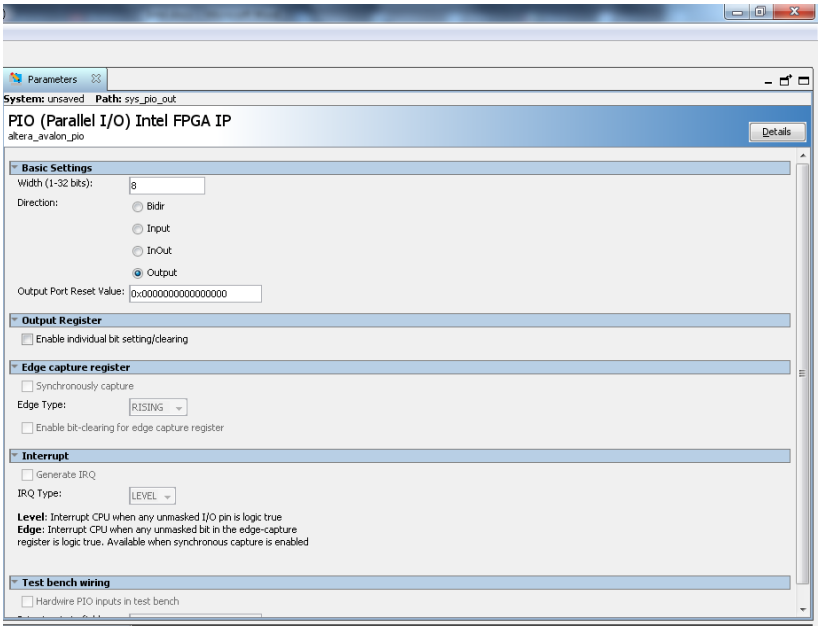
Identifier	Setting	Value
$system	**Clock crossing adapter type**	**Handshake**
$system	**Limit interconnect pipeline stages to**	**1**
$system	**Enable ECC protection**	**FALSE**
$system	**Automate default slave insertion**	**FALSE**

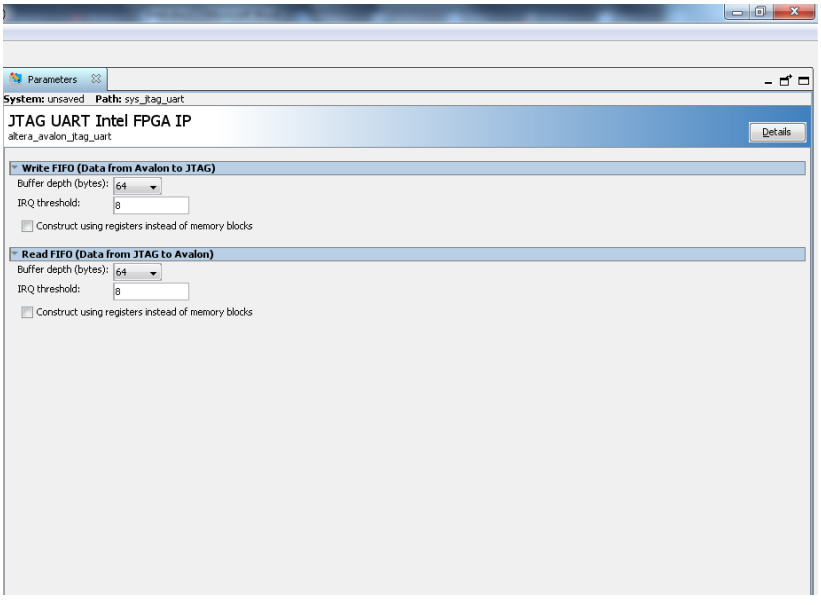
Messages

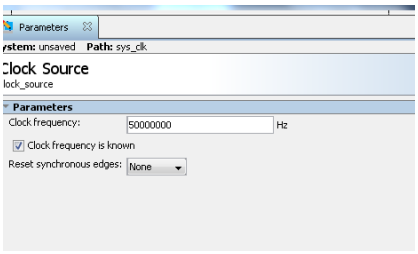
Type	Path	Message
2 Info Messages		
	unsaved.sys_jtag_uart	JTAG UART IP input clock need to be at least double (2x) the operating frequency of JTAG TCK on board
	unsaved.sys_pio_in	PIO inputs are not hardwired in test bench. Undefined values will be read from PIO inputs during simulation.

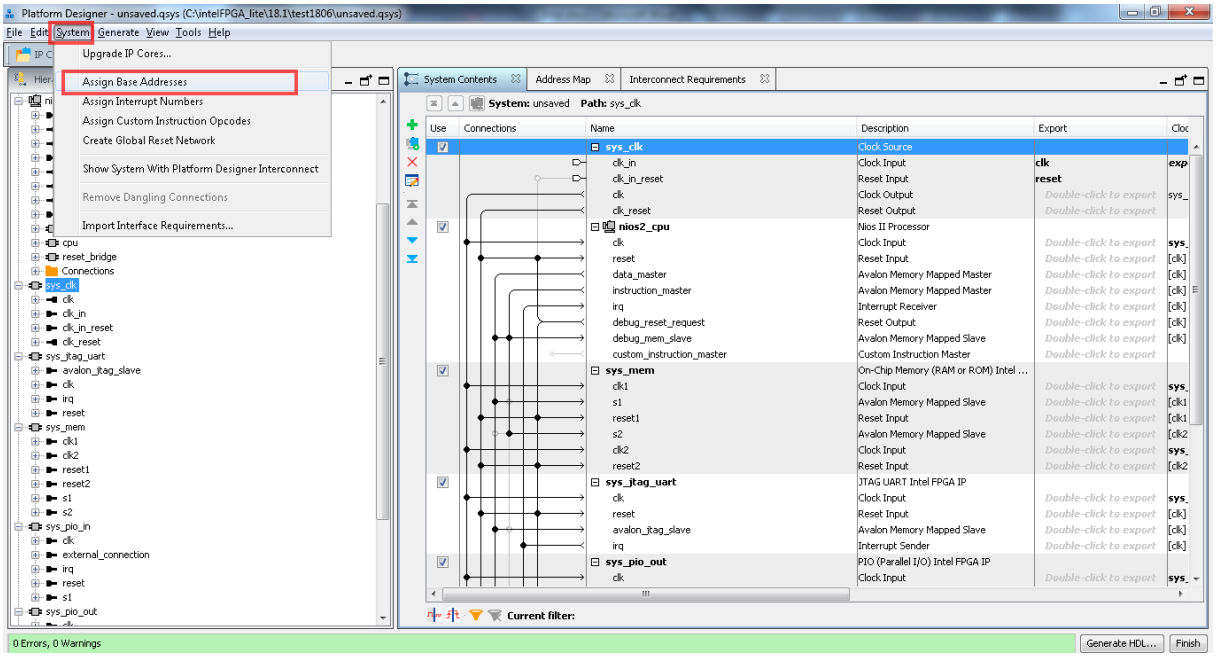


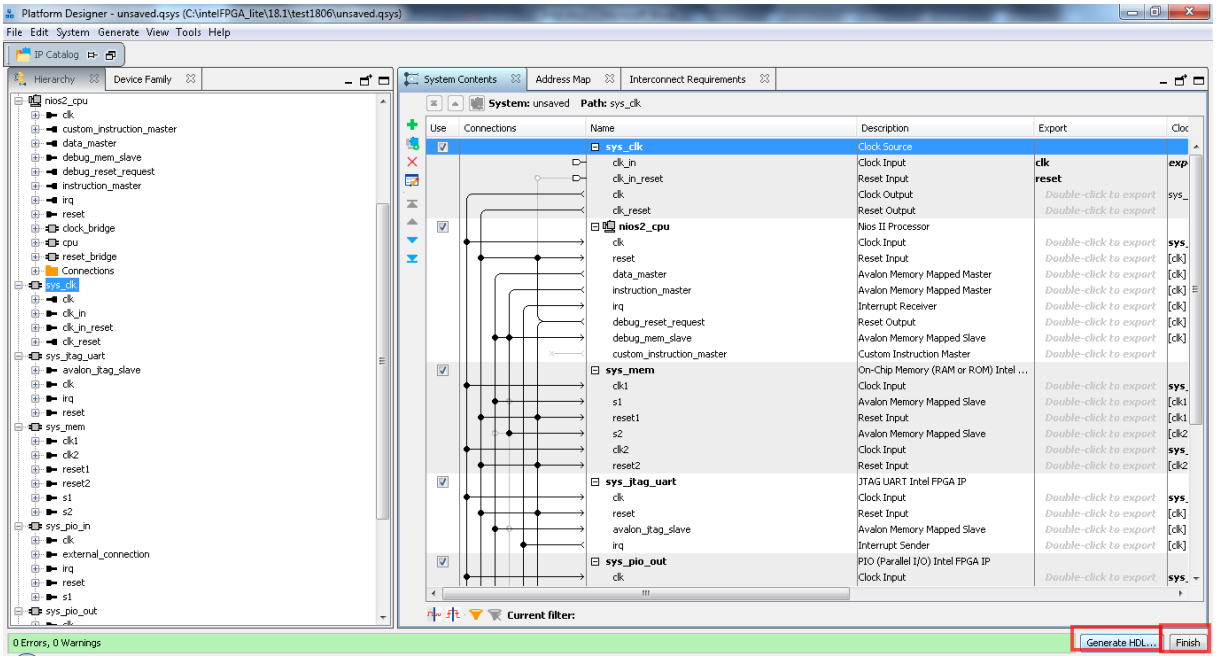

Parameters
System: unsaved Path: sys_pio_in
PIO (Parallel I/O) Intel FPGA IP
altera_avalon_pio
Details
Basic Settings
Width (1-32 bits): 1
Direction:
Bidir
Input
InOut
Output
Output Port Reset Value: 0x0000000000000000
Output Register
Enable individual bit setting/clearing
Edge capture register
Synchronously capture
Edge Type: RISING
Enable bit-clearing for edge capture register
Interrupt
Generate IRQ
IRQ Type: EDGE
Level: Interrupt CPU when any unmasked I/O pin is logic true
Edge: Interrupt CPU when any unmasked bit in the edge-capture register is logic true. Available when synchronous capture is enabled
Test bench wiring
Hardwire PIO inputs in test bench
VLC media player

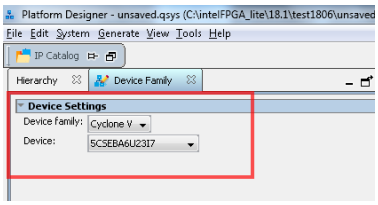

Parameters
System: unsaved Path: sys_pio_out
PIO (Parallel I/O) Intel FPGA IP
altera_avalon_pio
Details
Basic Settings
Width (1-32 bits): 8
Direction:
Bidir
Input
InOut
Output
Output Port Reset Value: 0x0000000000000000
Output Register
Enable individual bit setting/clearing
Edge capture register
Synchronously capture
Edge Type: RISING
Enable bit-clearing for edge capture register
Interrupt
Generate IRQ
IRQ Type: LEVEL
Level: Interrupt CPU when any unmasked I/O pin is logic true
Edge: Interrupt CPU when any unmasked bit in the edge-capture register is logic true. Available when synchronous capture is enabled
Test bench wiring
Hardwire PIO inputs in test bench

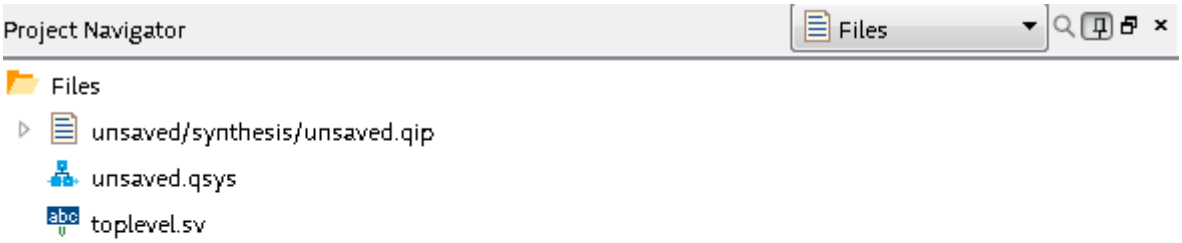

Parameters
System: unsaved Path: sys_jtag_uart
JTAG UART Intel FPGA IP
altera_avalon_jtag_uart
Details
Write FIFO (Data from Avalon to JTAG)
Buffer depth (bytes): 64
IRQ threshold: 8
Construct using registers instead of memory blocks
Read FIFO (Data from JTAG to Avalon)
Buffer depth (bytes): 64
IRQ threshold: 8
Construct using registers instead of memory blocks


Parameters
ystem: unsaved Path: sys_clk
Clock Source
lock_source
Parameters
Clock frequency:
50000000
Hz
Clock frequency is known
Reset synchronous edges:
None


Platform Designer - unsaved.qsys (C:\intelFPGA_lite\18.1\test1806\unsaved.qsys)
File Edit System Generate View Tools Help
Upgrade IP Cores...
Assign Base Addresses
Assign Interrupt Numbers
Assign Custom Instruction Opcodes
Create Global Reset Network
Show System With Platform Designer Interconnect
Remove Dangling Connections
Import Interface Requirements...
System Contents
Address Map
Interconnect Requirements
System: unsaved Path: sys_clk
Use
Connections
Name
Description
Export
sys_clk
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
clk
Clock Output
clk_reset
Reset Output
nios2_cpu
Nios II Processor
reset
data_master
Avalon Memory Mapped Master
instruction_master
irq
Interrupt Receiver
debug_reset_request
debug_mem_slave
Avalon Memory Mapped Slave
custom_instruction_master
Custom Instruction Master
sys_mem
On-Chip Memory (RAM or ROM) Intel ...
clk1
s1
reset1
s2
clk2
reset2
sys_jtag_uart
JTAG UART Intel FPGA IP
avalon_jtag_slave
sys_pio_out
PIO (Parallel I/O) Intel FPGA IP
Double-click to export
Current filter:
0 Errors, 0 Warnings
Generate HDL...
Finish


Platform Designer - unsaved.qsys (C:\intelFPGA_lite\18.1\test1806\unsaved.qsys)
File Edit System Generate View Tools Help
IP Catalog
Hierarchy
Device Family
nios2_cpu
clk
custom_instruction_master
data_master
debug_mem_slave
debug_reset_request
instruction_master
irq
reset
clock_bridge
cpu
reset_bridge
Connections
sys_clk
clk_in
clk_in_reset
clk_reset
sys_jtag_uart
avalon_jtag_slave
sys_mem
clk1
clk2
reset1
reset2
s1
s2
sys_pio_in
external_connection
sys_pio_out
System Contents
Address Map
Interconnect Requirements
System: unsaved Path: sys_clk
Use
Connections
Name
Description
Export
sys_clk
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
clk
Clock Output
clk_reset
Reset Output
nios2_cpu
Nios II Processor
reset
data_master
Avalon Memory Mapped Master
instruction_master
irq
Interrupt Receiver
debug_reset_request
debug_mem_slave
Avalon Memory Mapped Slave
custom_instruction_master
Custom Instruction Master
sys_mem
On-Chip Memory (RAM or ROM) Intel ...
clk1
s1
reset1
s2
clk2
reset2
sys_jtag_uart
JTAG UART Intel FPGA IP
avalon_jtag_slave
sys_pio_out
PIO (Parallel I/O) Intel FPGA IP
Double-click to export
Current filter:
0 Errors, 0 Warnings
Generate HDL...
Finish





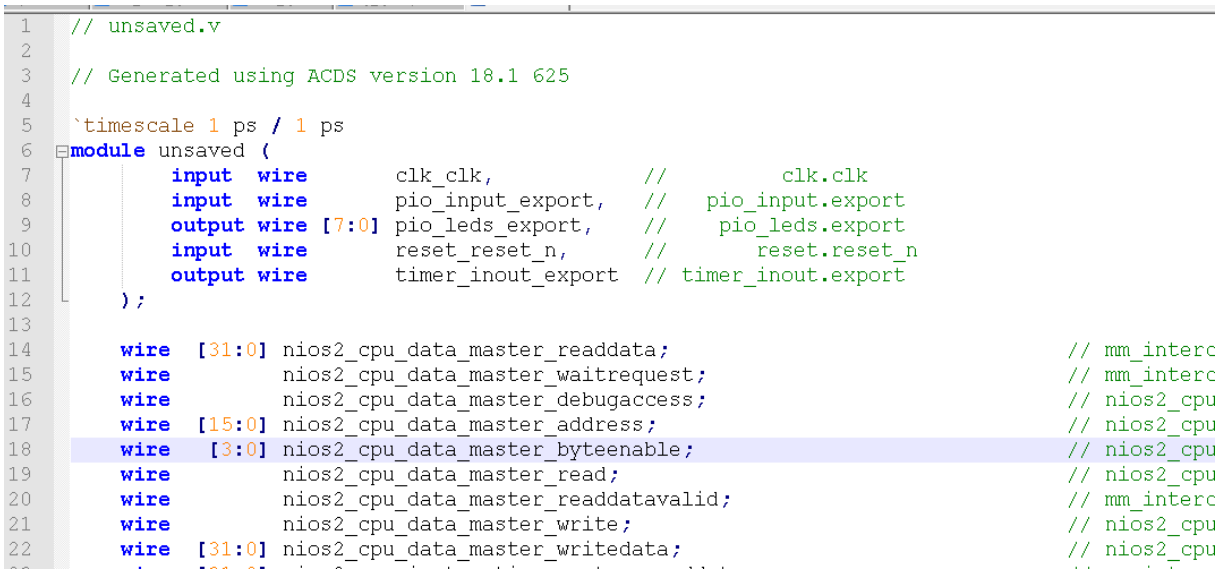
Toplevel

Instanciate a NIOS II

```
module toplevel( // hier muss der name vom TopLVL hin
// hier werden die signale den realen PINS auf dem Cyclone V zugewiesen, kann man auch im
    (* chip_pin = "V11" *) input logic clk,
    (* chip_pin = "AH17"  *) input logic reset_n,
    (* chip_pin = "AA23, V12, AE26, AF26, V15, V16, AA24, W15" *) output logic [7:0] q
    );

    unsaved base_sys (.clk_clk(clk), // hier wird dann das ganze zeug was im Plattform Desi
    //erstellt wurde isntanziiert. das module fndet man auch in der .qip
    //sammlung. qip bdeuet Quartus IP . die erste datei ist es . in diesem fall "unsaved.v"
                      .reset_reset_n(reset_n),
                      .pio_leds_export(q)
    );


endmodule
```

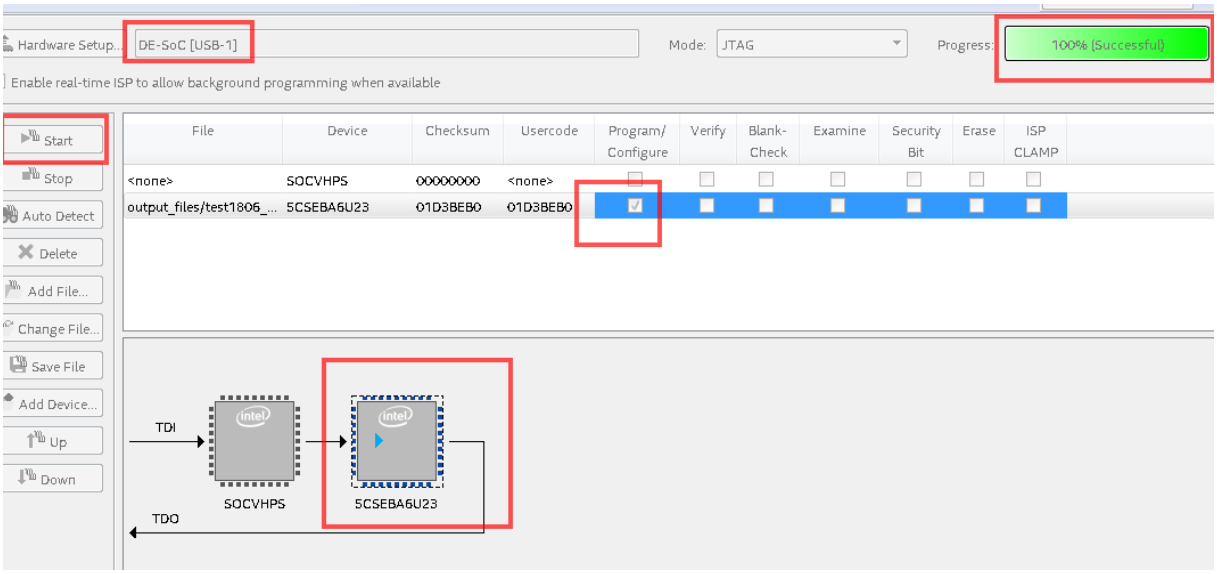


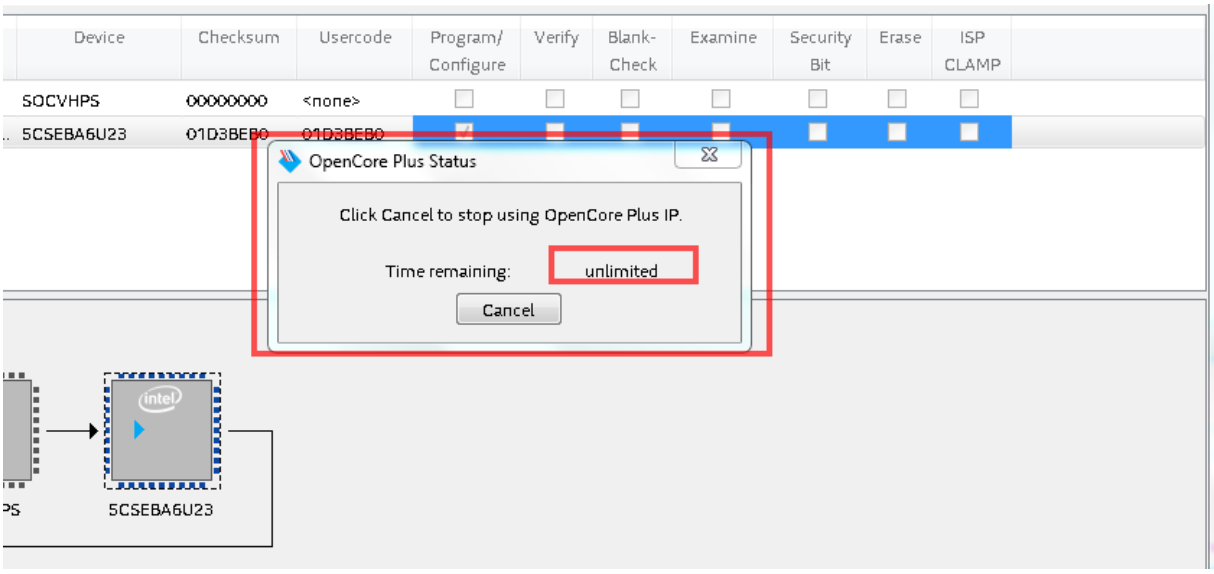
```
1  // unsaved.v
2
3  // Generated using ACDS version 18.1 625
4
5  `timescale 1 ps / 1 ps
6  module unsaved (
7          input  wire       clk_clk,            //         clk.clk
8          input  wire       pio_input_export,   //   pio_input.export
9          output wire [7:0] pio_leds_export,    //    pio_leds.export
10         input  wire       reset_reset_n,      //       reset.reset_n
11         output wire       timer_inout_export  // timer_inout.export
12     );
13
14     wire  [31:0] nios2_cpu_data_master_readdata;                    // mm_interc
15     wire         nios2_cpu_data_master_waitrequest;                 // mm_interc
16     wire         nios2_cpu_data_master_debugaccess;                 // nios2_cpu
17     wire  [15:0] nios2_cpu_data_master_address;                     // nios2_cpu
18     wire   [3:0] nios2_cpu_data_master_byteenable;                  // nios2_cpu
19     wire         nios2_cpu_data_master_read;                        // nios2_cpu
20     wire         nios2_cpu_data_master_readdatavalid;               // mm_interc
21     wire         nios2_cpu_data_master_write;                       // nios2_cpu
22     wire  [31:0] nios2_cpu_data_master_writedata;                   // nios2_cpu
```

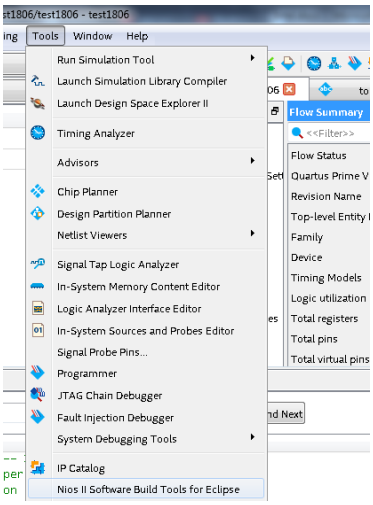
Warnings when compiling

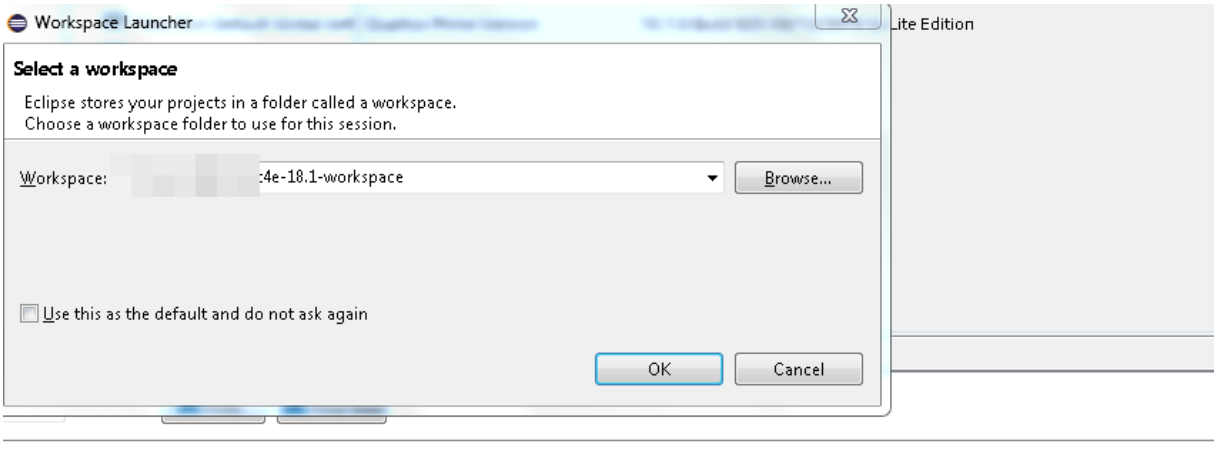
Warning (18236): Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
Warning (12020): Port "jdo" on the entity instantiation of "the_unsaved_nios2_cpu_cpu_nios2_oci_itrace" is connected to a signal of width 38. The formal width of the signal in the module is 16. The extra bits will be ignored.
Warning (12188): Intel FPGA IP Evaluation Mode feature is turned on for the following cores
Warning (12190): "Nios II Processor (6AF7_00A2)" will use the Intel FPGA IP Evaluation Mode feature
Warning (12190): "Nios II Processor (6AF7_00A2)" will use the Intel FPGA IP Evaluation Mode feature
Warning (265072): Messages from megafunction that supports Intel FPGA IP Evaluation Mode feature
Warning (265073): Messages from megafunction that supports Intel FPGA IP Evaluation Mode feature Nios II Processor
Warning (265074): The reset input will be asserted when the evaluation time expires
Warning (265073): Messages from megafunction that supports Intel FPGA IP Evaluation Mode feature Nios II Processor
Warning (265074): The reset input will be asserted when the evaluation time expires
Warning (265074): The reset input will be asserted when the evaluation time expires
Warning (265069): Megafunction that supports Intel FPGA IP Evaluation Mode feature will stop functioning in 1 hour after device is programmed
Warning (12241): 3 hierarchies have connectivity warnings - see the Connectivity Checks report folder
Warning (18236): Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
Warning (292013): Feature LogicLock is only available with a valid subscription license. You can purchase a software subscription to gain full access to this feature.
Warning (15714): Some pins have incomplete I/O assignments. Refer to the I/O Assignment Warnings report for details

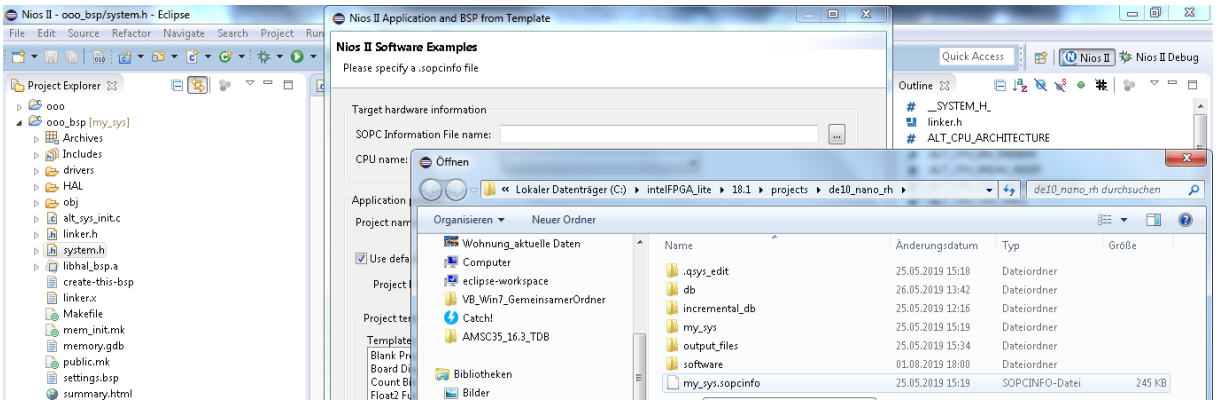
Warning (18236): Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
Warning (210042): Can't convert time-limited SOF into POF, HEX File, TTF, or RBF
Warning (18236): Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.



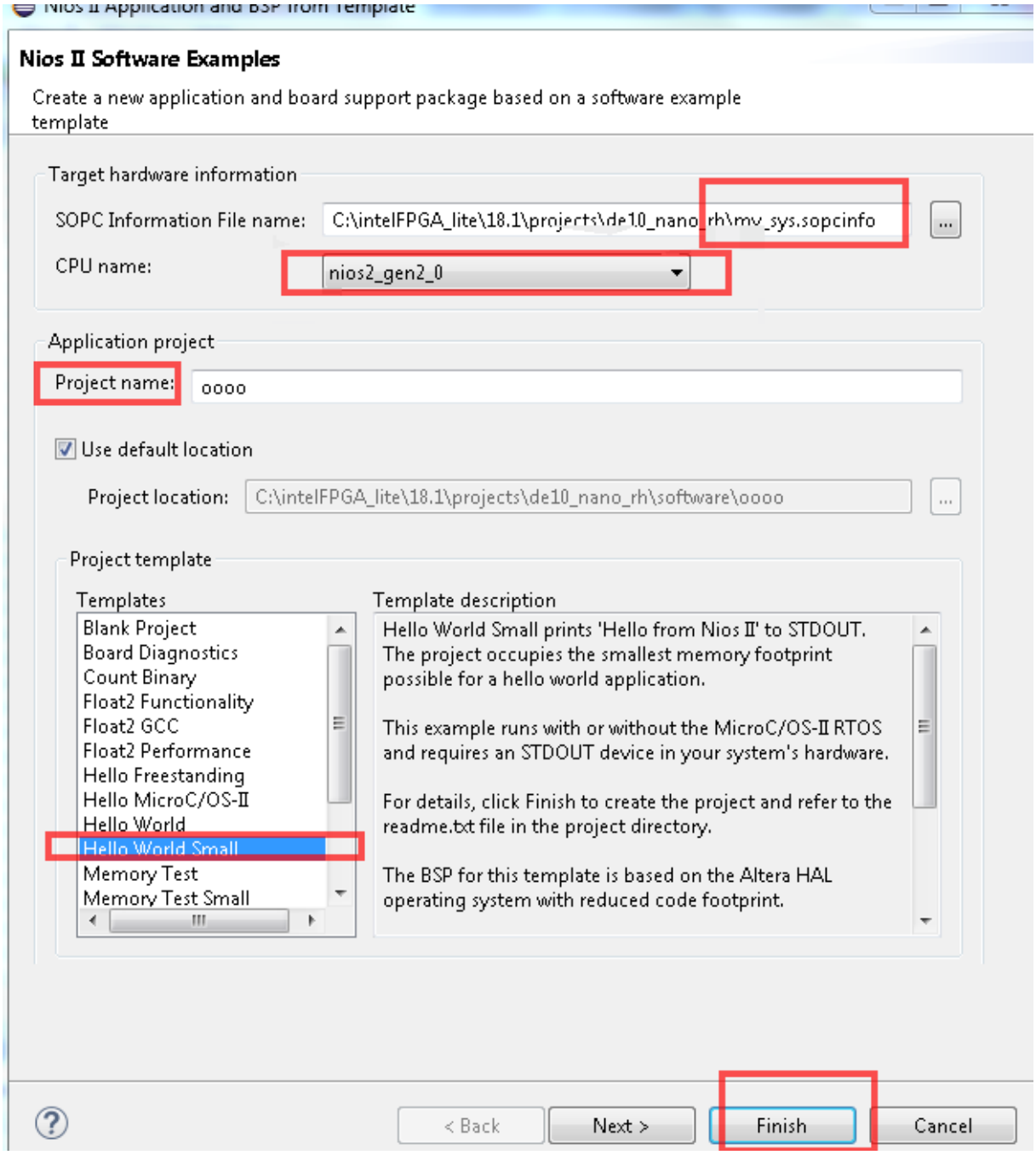


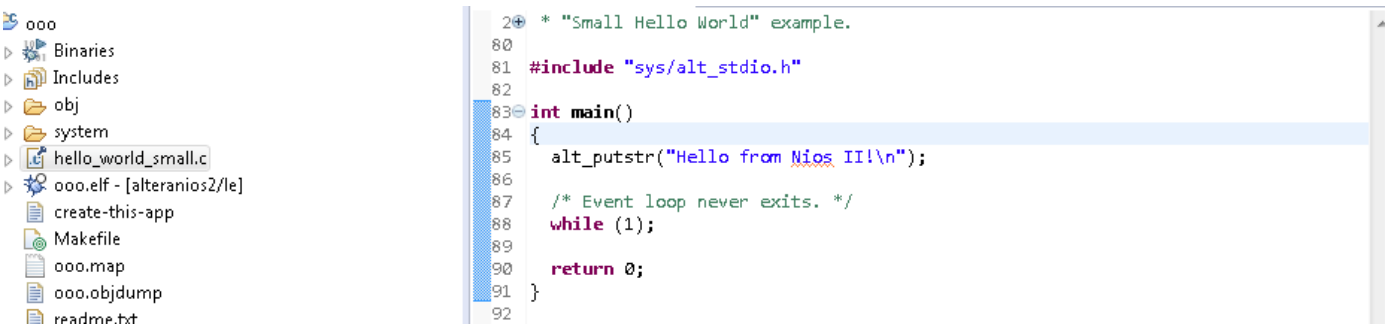

Tools
Window
Help
Run Simulation Tool
Launch Simulation Library Compiler
Launch Design Space Explorer II
Timing Analyzer
Advisors
Chip Planner
Design Partition Planner
Netlist Viewers
Signal Tap Logic Analyzer
In-System Memory Content Editor
Logic Analyzer Interface Editor
In-System Sources and Probes Editor
Signal Probe Pins...
Programmer
JTAG Chain Debugger
Fault Injection Debugger
System Debugging Tools
IP Catalog
Nios II Software Build Tools for Eclipse
Flow Summary

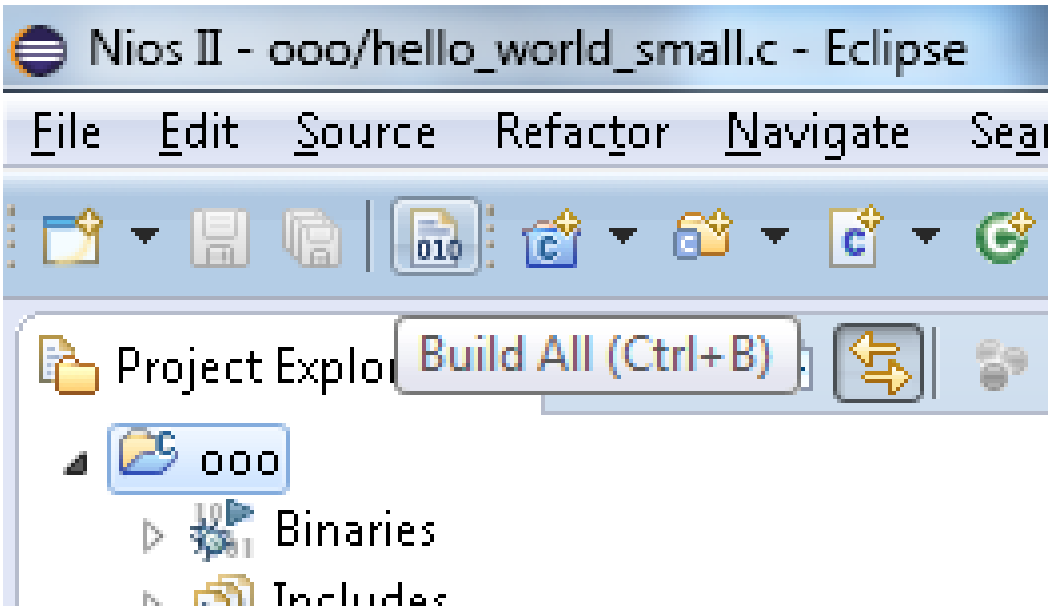

Workspace Launcher
Select a workspace
Eclipse stores your projects in a folder called a workspace.
Choose a workspace folder to use for this session.
Workspace:
Browse...
Use this as the default and do not ask again
OK
Cancel

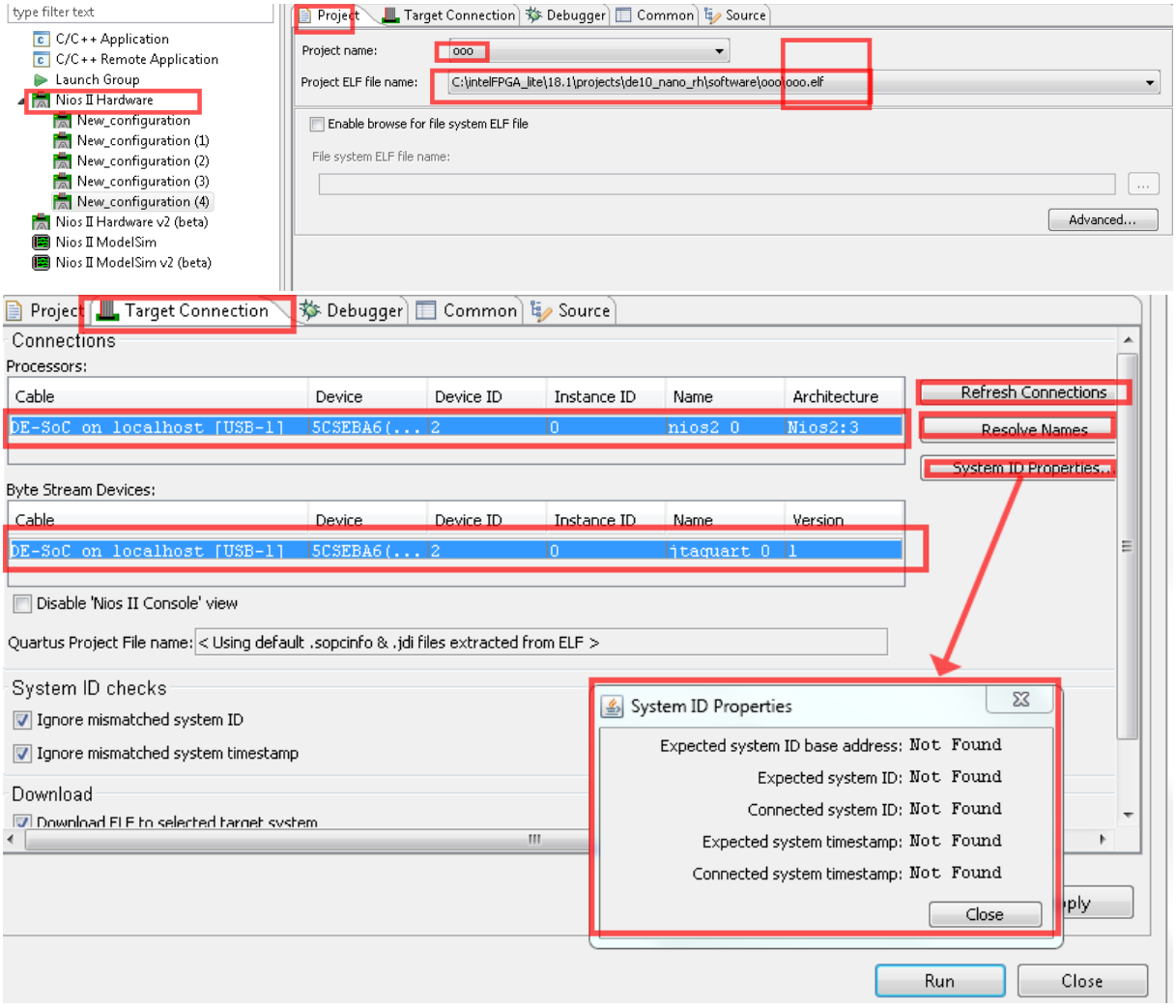

Nios II - ooo_bsp/system.h - Eclipse
Nios II Application and BSP from Template
Nios II Software Examples
Please specify a .sopcinfo file
Target hardware information
SOPC Information File name:
CPU name:
Öffnen
Project Explorer
Outline
Organisieren
Neuer Ordner
my_sys.sopcinfo

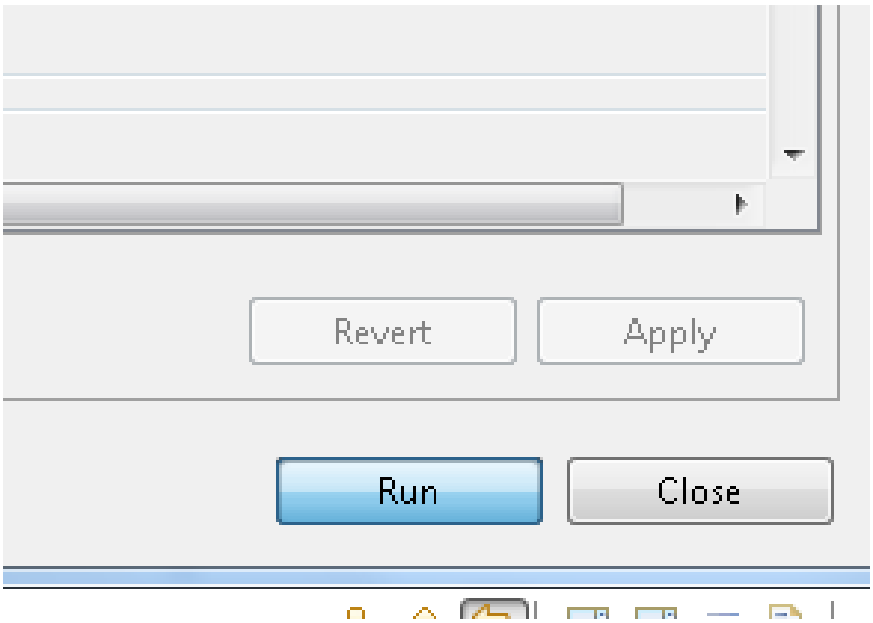
#


Nios II Application and BSP from Template
Nios II Software Examples
Create a new application and board support package based on a software example template
Target hardware information
SOPC Information File name: C:\intelFPGA_lite\18.1\projects\de10_nano_rh\my_sys.sopcinfo
CPU name: nios2_gen2_0
Application project
Project name: oooo
Use default location
Project location: C:\intelFPGA_lite\18.1\projects\de10_nano_rh\software\oooo
Project template
Templates
Blank Project
Board Diagnostics
Count Binary
Float2 Functionality
Float2 GCC
Float2 Performance
Hello Freestanding
Hello MicroC/OS-II
Hello World
Hello World Small
Memory Test
Memory Test Small
Template description
Hello World Small prints 'Hello from Nios II' to STDOUT. The project occupies the smallest memory footprint possible for a hello world application.
This example runs with or without the MicroC/OS-II RTOS and requires an STDOUT device in your system's hardware.
For details, click Finish to create the project and refer to the readme.txt file in the project directory.
The BSP for this template is based on the Altera HAL operating system with reduced code footprint.
< Back
Next >
Finish
Cancel


ooo
Binaries
Includes
obj
system
hello_world_small.c
ooo.elf - [alteranios2/le]
create-this-app
Makefile
ooo.map
ooo.objdump
readme.txt
* "Small Hello World" example.
#include "sys/alt_stdio.h"
int main()
{
alt_putstr("Hello from Nios II!\n");
/* Event loop never exits. */
while (1);
return 0;
}


Nios II - ooo/hello_world_small.c - Eclipse
File Edit Source Refactor Navigate Sea
Project Explo
Build All (Ctrl+B)
ooo
Binaries


type filter text
C/C++ Application
C/C++ Remote Application
Launch Group
Nios II Hardware
New_configuration
New_configuration (1)
New_configuration (2)
New_configuration (3)
New_configuration (4)
Nios II Hardware v2 (beta)
Nios II ModelSim
Nios II ModelSim v2 (beta)
Project
Target Connection
Debugger
Common
Source
Project name:
ooo
Project ELF file name:
C:\intelFPGA_lite\18.1\projects\de10_nano_rh\software\ooo\ooo.elf
Enable browse for file system ELF file
File system ELF file name:
Advanced...
Connections
Processors:
Cable
Device
Device ID
Instance ID
Name
Architecture
DE-SoC on localhost [USB-1]
5CSEBA6(...
2
0
nios2_0
Nios2:3
Refresh Connections
Resolve Names
System ID Properties...
Byte Stream Devices:
Version
jtaguart_0
1
Disable 'Nios II Console' view
Quartus Project File name:
< Using default .sopcinfo & .jdi files extracted from ELF >
System ID checks
Ignore mismatched system ID
Ignore mismatched system timestamp
Download
System ID Properties
Expected system ID base address: Not Found
Expected system ID: Not Found
Connected system ID: Not Found
Expected system timestamp: Not Found
Connected system timestamp: Not Found
Close
Run
Close



Console | Nios II Console | Properties | Search

<terminated> New_configuration (4) [Nios II Hardware] nios2-download (01.08.19, 20:01)

```
Using cable "DE-SoC [USB-1]", device 2, instance 0x00
Pausing target processor: OK
Initializing CPU cache (if present)
OK

Downloading 00000000 (  0%)
Downloading 000002FC ( 99%)
Downloaded 1KB in 0.0s

Verifying 00000000 (  0%)
Verifying 000002FC ( 99%)
Verified OK
Starting processor at address 0x00000020
```