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AMD Tackles Coming "Chiplet" Revolution With New Chip Network Scheme

Active silicon interposers could make for smaller, better computers but the networks need to mesh

By **Samuel K. Moore (/author/moore-samuel-k)**

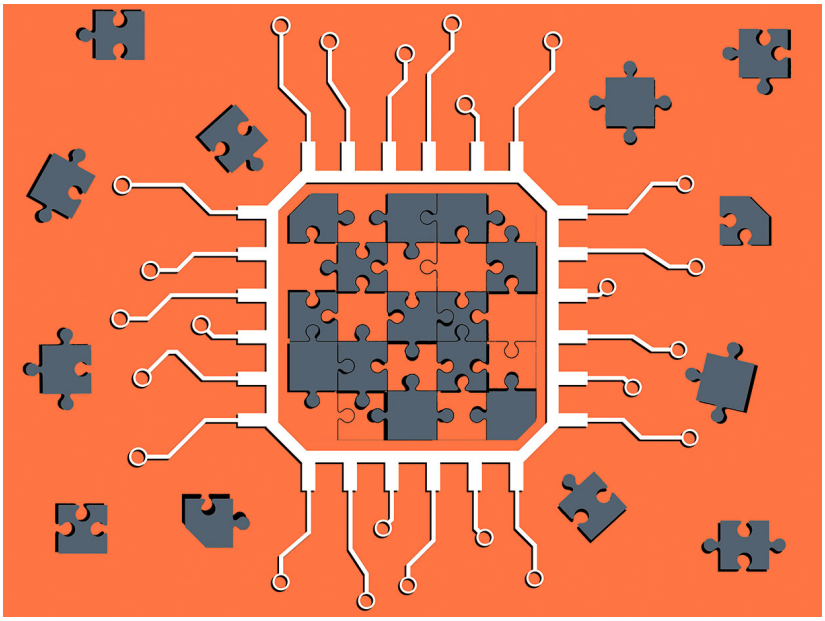

Illustration: iStockphoto/IEEE Spectrum

The time may be coming when computers and other systems are made not from individually packaged chips attached to a printed circuit board but from bare ICs interconnected on a larger slice of silicon. Researchers have been developing this concept called "chiplets (/nanoclast/computing/hardware/4-strange-new-ways-to-make-a-computer)" with the idea that it will let data move faster and freer to make smaller, cheaper, and more tightly integrated computer systems. The idea is that individual CPUs, memory, and other key systems can all be mounted onto a relatively large slice of silicon, called an active interposer, which is thick with interconnects and routing circuits.

"In some sense if this were to pan out it's somewhat similar to the integration story—Moore's Law and everything else—that we've been writing for decades," says Gabriel Loh, Fellow Design Engineer at AMD (http://ir.amd.com/news-releases/news-release-details/amd-engineer-gabriel-loh-named-2018-maurice-wilkes-award-winner). "It allows the industry to take a variety of system components and integrate them more compactly and more efficiently together."

There's (at least) one problem: Though each chiplet's own on-chip routing system can work perfectly, when they're all connected together on the interposer's network a situation can arise where a network tries to route data in such a way that a traffic jam occurs that winds up seizing up the computer. "A deadlock can happen basically where you have a circle or a cycle of different messages all trying to compete for same sorts of resources causing everyone to wait for everyone else," Loh explains.

“Each of those individual [chiplets] could be designed so that they never have deadlocks,” says Loh. “But once I put them together, there are now new paths and new routes that no individual had planned for ahead of time.” Trying to avoid these new deadlocks by designing all the chiplets together with a particular interposer network in mind would defeat the advantages of the technique: Chiplets, then, couldn’t be designed and optimized easily by separate teams, and they couldn’t easily be mixed and matched to quickly form new systems. At the International Symposium on Computer Architecture (http://iscaconf.org/isca2018/index.html)earlier this month, engineers at AMD presented a potential solution to this impending problem.

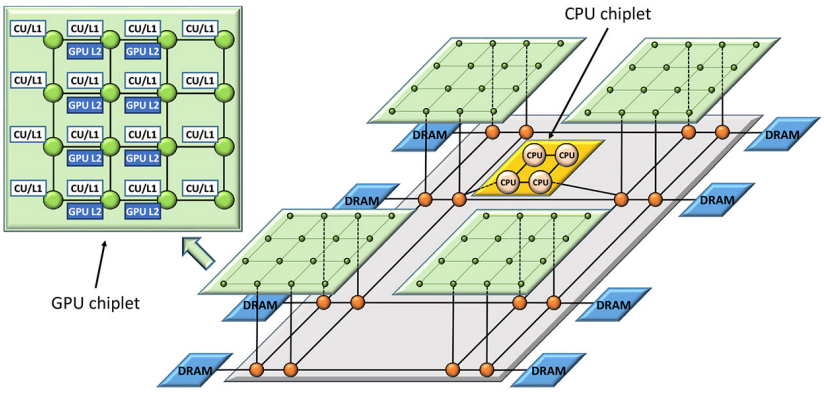

Illustration: AMD

A future system might contain a CPU chiplet and several GPUs all attached to the same piece of network-enabled silicon.

The AMD team found that deadlocks on active interposers basically disappear if you follow a few simple rules when designing on-chip networks. These rules govern where data is allowed to enter and leave the chip and also restricts which directions it can go when it first enters the chip. Amazingly, if you follow those rules you can pretend everything else on the interposer—all the other logic chiplets, memory, the interposer’s own network, everything—is just one node on the network. Knowing that, separate teams of engineers can design chiplets without having to worry about how the networks on other chiplets work or even how the network on the active interposer works.

It may be some time before this trick is even needed. So-called passive interposers—silicon that contains interconnects but no network circuits—are already in use; AMD has been using one for its Radeon R9 (https://www.amd.com/en-us/products/graphics/desktop/r9) series, for example. But adding an intelligent network to the interposer could lead to a big change in how systems are designed and what they can do.

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